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13. ABSTRACT (Maximum 200 Words) The research performed under this grant was focused on two aspects of GaN-dielectric interfaces: i) the development of remote plasma processing to yield device quality interfaces suitable for applications including metal oxide semiconductor (MOS) devices, as well surface passivation for high electron mobility transistor (HEMT) devices, and ii) determination of band offset energies between GaN and dielectrics including silicon dioxide (SiO ₂), silicon nitride (Si ₃ N ₄) and a representative high-k alternative dielectric, hafnium oxide (HfO ₂). Considerable progress was made in each of these areas, and the research has been documented in numerous publications. In particular, a low temperature (300°C) remote plasma processing sequence was developed which minimized interfacial traps (d _{it}), and identified the importance of self-organized gallium suboxide, (GaO _x , x<1.5) interfacial layers. Conduction band offset energies between GaN and the representative dielectrics studied were adequate for MOS and surface passivation applications. The critical nature of the self-organized GaO _x layer was verified by showing that interfaces with thicker layers, ~1.5 nm as contrasted with ~0.8 nm, yielded increased densities of interfacial defects, attributed to the inability balance bond and macroscopic strain.					
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Technical Report

1. Introduction

The primary research objective of this proposal is to prepare and characterize low defect density interfaces between i) GaN and other groups III nitrides, that can be extended to their pseudo-binary and ternary alloys with In and Al, and ii) gate dielectric materials including SiO_2 , silicon nitride, silicon oxynitride alloys and the high-k oxides and silicates being developed for aggressively-scaled Si field effect transistors (FETs). These GaN interfaces would then be incorporated into device structures in several different ways; i) as gate dielectric layers in FET devices, ii) as surface passivation layers in high electron mobility transistors (HEMTs), and photo-devices including photo-detectors, and electroluminescent devices.

Two research students have contributed to the effort, Choelhwyl Bae and Ted Cook. Each of these students completed his PhD requirements, during the past two months, Dr. Bae in the Department of Electrical and Computer Engineering, under the supervision of Professor Gerald Lucovsky of the Department of Physics, and Dr. Cook, under the supervision of Professor Robert J. Nemanich of the Department of Physics, in the Department of Materials Science and Engineering. The research projects of these students focused on complementary aspects of the research task: i) Choelhwyl Bae developed a remote plasma processing to yield device quality interfaces suitable for applications including metal oxide semiconductor (MOS) devices, as well surface passivation for high electron mobility transistor (HEMT) devices, and ii) Ted Cook determined band offset energies between GaN and dielectrics including silicon dioxide (SiO_2), silicon nitride (Si_3N_4) and a representative high-k alternative dielectric, hafnium oxide (HfO_2).

The remainder of the report discusses the results. It is divided into three sections; the first deals with plasma processing, the second with new and important insights into suboxide regions between semiconductors and dielectrics, and the third with the band offset energy determinations.

2. Remote plasma processing

Figures 1 and 2 display respectively, the multi-chamber remote plasma processing system used for the processing studies, and remote plasma processing chamber. GaN samples were placed in the load lock chamber after ex-situ wet cleans, and then transported into the plasma processing chamber, where plasma cleaning, remote plasma assisted oxidation (RPAO) and nitridation (RPAN), and remote plasma enhanced chemical vapor deposition (RPECVD) steps were performed. Remote plasma processing could be interrupted so that samples could be transported under ultra high vacuum base pressures to the analysis chamber where chemical analysis by Auger

electron spectroscopy (AES) could be performed. This is aspect of interrupted processing and analysis was the capability of the multi-chamber system that enabled use to monitor and understand the processing steps with a resolution of ~ 0.6 nm.

2.1 Ex-situ cleaning and N₂ plasma in-situ clean.

As received GaN epitaxial layers on sapphire substrates were subjected to ex-situ chemical cleans using different etching solutions. The results of these studies are summarized in Fig. 3. The epitaxial GaN (0001) layers were directly grown on the *c*-plane of sapphire by hydride vapor phase epitaxy (HVPE). Silicon was used as *n*-type dopant, and the thickness of the GaN epitaxial layer was 5 μm . These GaN layers had an electron concentrations of $5\text{--}10 \times 10^{17} \text{ cm}^{-3}$. The 2-inch GaN/sapphire wafers were degreased in acetone, and then methanol, each for 20 minutes. A standard RCA clean was followed by etching in several different solutions identified in Fig. 3 at 90°C. Following this, GaN samples were loaded into a multi-chamber system which provided chambers for remote plasma-assisted processing and on-line AES measurements. There were essentially no differences in the chemical quality of the GaN surface following any of these procedures. However, subsequent studies indicated that the density of interfacial defects could be reduced by following an RPAO step, rather than proceeding it, and this is the then the processing that has been found to be optimum for GaN dielectric interfaces using the remote plasma processing approach of this program.

2.2 Optimized remote plasma processing

In our initial studies of GaN-dielectric interfaces, it had been demonstrated that an RPAO step prior to SiO₂ deposition by RPECVD reduced interface traps, D_{it} , by more than a factor of five [1], from more than 10^{12} cm^{-2} to $> 5 \times 10^{11} \text{ cm}^{-2}$. However, a D_{it} of $> 5 \times 10^{11} \text{ cm}^{-2}$ was still too high, for many MOS devices, as well as for surface passivation of HEMT devices as.. Analysis by on-line Auger electron spectroscopy, AES, showed that the RPAO step formed an ultra-thin $\sim 0.5\text{--}0.6$ nm layer of GaO_{*x*} with $x \sim 1.5$, and additionally prevented subcutaneous oxidation of the GaN substrate during an RPECVD deposition of SiO₂. These two aspects of the RPAO step are similar to the formation of device quality Si-SiO₂ hetero-structures by low temperature plasma processing [2]. For applications to GaN, the pre-RPAO surface preparation processing included: i) a chemical wet clean, with equivalent results using the etch baths described above, and ii) a remote plasma N₂ clean that reduced the residual oxygen atom concentration at the GaN surface. The plasma N₂ clean was suggested by the use of high temperature, 800°C, NH₃ cleaning step prior to the formation of GaN-(In,Ga)N or (Al,Ga)N hetero-structures [3]. As noted above, it was shown that reversing the order of the N processing steps, i.e., following the RPAO by an RPAN step, rather than preceding it by an N₂ plasma clean, yielded lower densities of interfacial defects. The lower traces in Fig. 3 demonstrates that the degree of surface cleaning is essentially independent of the particular etchant used. Figs. 4(a) and (b) present the RPAO

oxidation kinetics as determined from analysis by on-line AES. The data points in Figs. 4(a) and (b) were obtained by interrupted processing and AES analysis.

The GaN/sapphire wafers were degreased in acetone, and then methanol, each for 20 minutes. A standard RCA clean was followed by etching in 1:5 $\text{NH}_4\text{OH}:\text{H}_2\text{O}$ solutions at 60-90°C (or in HCl based solutions, See Fig. 3). Following this, GaN samples were loaded into a multi-chamber system, which provided chambers for remote plasma-assisted processing and on-line AES measurements. In our previously reported work, the GaN wafer was first exposed to reactive species from a remote N_2/He discharge at 0.02-0.3 Torr for an in-situ clean that removed Cl, C and O surface contaminants. The *in situ* cleaned GaN surface was then oxidized by an RPAO process using a He/O_2 source gas mixture. For the SiO_2 deposition, the flow rates for plasma excited O_2 and He, and down-stream injected 2%- SiH_4 in He were respectively 60, 200 and 10 sccm. The process pressure, substrate temperature and plasma power for both the oxidation and SiO_2 deposition were respectively 0.3 Torr., 300°C and 30 W at 13.56 MHz. Post oxide deposition annealing (POA) was carried out at 900°C for 30 min in an N_2 atmosphere. For the fabrication of GaN MOS capacitors, a 300 nm Al layer was evaporated after the formation of the gate dielectric. After an electrode area was defined by a conventional lithography process, post metallization annealing (PMA) was performed at 400°C for 30 min in forming gas (N_2/H_2).

As noted above, it was subsequently found that additional reductions in D_{it} to the low 10^{11} cm^{-2} regime by two processing sequence modifications. The first was the elimination of the pre-RPAO, N_2 plasma clean. The rationale for this was that in the formation of device-quality Si-SiO₂ interfaces by remote plasma processing, the RPAO step performed two functions: i) it reduced the number of surface contaminants, such as Cl and F, from pre-deposition wet chemical cleaning (e.g., an RCA clean followed by a rinse in dilute HF), and ii) it formed a chemical oxide that prevented subcutaneous oxidation of the Si substrate during the SiO_2 deposition step. Therefore it was not obvious that the remote plasma clean was need. The second was the insertion of an RPAO step after the RPAO. This sequence, RPAO followed by RPAO, reduced direct tunneling and improved reliability at Si-SiO₂ interfaces [4]. Another process variation was used in which a combined RPAO/RPAO step was performed by replacing the O_2/He mixture of the RPAO step with an $\text{N}_2\text{O}/\text{He}$ mixture. This single step oxidation, interface nitridation process had also yield improvements in reliability at the nitrided Si-SiO₂ interfaces.

Interfacial bonding changes and the development of GaO_x and SiO_2 dielectrics were monitored by on-line AES. Figures 4(a) and (b) compare the growth rates for interfacial GaO_x using the O_2/He and $\text{N}_2\text{O}/\text{He}$ processes. The reduction of the oxidation rate for the N_2O process parallels what was found for the same processes applied to Si. Figure 5 demonstrates that an RPAO process preceding RPECVD deposition of SiO_2 eliminates subcutaneous oxidation during the RPECVD process. Analysis of C-V traces

with and without RPAO steps demonstrated order of magnitude reductions in D_{it} when the RPAO step was employed.

2.3 Interface electrical properties

Figures 6 and 7 demonstrate that the following a wet chemical clean in NH_4OH , a pre-deposition RPAO step significantly reduces interface trapping. The resulting C-V characteristics further demonstrated that the density of interface traps, monitored by analysis of frequency dependent C-V trace differences, was reduced below the level of what was obtained using the plasma N_2 clean step. Figures 6(a) and (b) demonstrate further reductions in frequency dispersion and D_{it} obtained by optimization of a RPAN step following the RPAO. Included in the comparisons is a processing in which the RPAO step is performed with N_2O as the source gas. In studies of Si-SiO₂ interface formation, the use of N_2O had been demonstrated to provide mono-layer interface nitridation during the RPAO step. The comparisons in Figs. 6 and 7 are summarized in Fig. 8 and demonstrate similar D_{it} values for RPAO using O_2 and N_2O , but additional reductions in D_{it} by following the RPAO step with the RPAN process step, i.e., by separate steps for forming an interfacial oxide, and nitriding the GaN-oxide interface after its creation. Fig. 9(a) demonstrates the quality of the fit to the C-V characteristic, and more importantly that GaN devices go into deep depletion (see Fig. 9(b)) as the negative bias on the gate electrode is increased. This is due to a very low generation rate for minority carriers.

These results demonstrate that as in studies of plasma processed Si-SiO₂ interfaces, interface nitridation by insertion of an RPAN step after the RPAP yields the best results. They also demonstrate that a plasma cleaning step, prior to RPAO resulted in poor interface performance. A similar observation had been made for processing of Si-SiO₂ interfaces, where an H_2/He plasma clean prior to the RPAO step yielded poorer interface properties compared to the elimination of the pre-RPAO H_2/He clean, and the insertion of the plasma N_2/He nitridation improved interface performance. In contrast to the studies of plasma-nitrided SiO₂ interfaces, changes in the bonding at GaN-GaO_x interfaces could not be monitored by studying changes in the N 1s Auger feature.

3. Interfacial suboxide regions: *an important insight into semiconductor dielectric interfaces*

This section of the report provides new insights in the relaxation of localized bond strain, and macroscopic stress at Si-SiO₂ interfaces, which are applicable to GaN-dielectric interfaces as well. The motivation for revisiting some of the previous results on the application of optical second harmonic generation (SHG) to probe these interfaces will become apparent as the results are examined in the context of important new insights into changes in bonding that occur in the transition region between the crystalline Si substrate and a thin film dielectric such as SiO₂. It is well established that

Si-SiO₂ interfaces in metal-oxide-semiconductor field effect transistor (MOSFET) devices are not atomically abrupt, but instead contain i) a transition region ~0.5 nm thick in which the distribution of local bonding arrangements have average SiO composition, as well as ii) a strained or *defective* region in the Si substrate that is of similar spatial extent and that likely also contains Si dangling bonds [5-13]. Similar interfacial transition regions have been identified at interfaces between Si and high-k dielectrics [7]. It is therefore critically important to understand i) the basic physical and chemical forces that drive the creation of these regions, ii) the bonding within these regions, and iii) the effects that these different regions have on device performance and reliability. This paper addresses these issues through new and important insights into the nature of self-organized regions that are known to develop at *compositional* interfaces between unconstrained and heavily constrained materials; i.e., the Si and SiO₂ of the Si-SiO₂ interface structure. This is accomplished through i) studies of bonding at Si-SiO₂ interfaces by (a) spectroscopic and single wavelength ellipsometry [8,9], (b) optical second harmonic generation [10-12], (c) synchrotron x-ray photoelectron spectroscopy and (d) ion scattering [5,13], and ii) by comparisons with non-crystalline glass alloy systems such as Ge_xSe_{1-x} which span a range of under-constrained or *floppy* bonding arrangements ($x < 0.2$) to over-constrained or *rigid* bonding arrangements ($x > 0.25$) [14].

Three factors contribute to the formation of transition regions at Si-SiO₂ interfaces: i) differences in Si-Si inter-atomic-distances in the Si substrate (0.235 nm) and the SiO₂ dielectric (~0.305 nm) that result in intrinsic compressive stress in the oxide and tensile stress in the substrate, ii) differences in linear thermal expansion coefficients in the SiO₂ dielectric ($0.5 \times 10^{-6} \text{ C}^{-1}$) and the Si substrate ($2.5 \times 10^{-6} \text{ C}^{-1}$) that contribute a thermally-induced stress component, and iii) differences in the average number of bonds per atom, 4 in the substrate, and 2.7 in the SiO₂ film that contribute to bond-strain at the atomic scale. Relevant experimental results for Si-SiO₂ interfaces are first summarized, and then discussed in the context of physical and chemical bonding mechanisms. The emphasis is then shifted to gate dielectric interface integrity at a microscopic bonding level that is extended from Si-SiO₂ interfaces, Si-high-k dielectric interfaces and GaN dielectric interfaces as well.

3.1 Experimental Results

3.1.1 medium energy ion scattering

Studies of medium ion energy scattering identified SiO_x and defective Si interfacial regions ~0.5 nm thick at Si-SiO₂ interfaces [5,13]. These experiments were done in a channeling direction on Si(111) substrates using He⁺ ions and detecting ion scattering out of these beams at angles greater than 70 degrees. The scattering was studied as a function of the SiO₂ layer thickness, and compared with models that included a strained or defect layer with the Si substrate at the interface, denoted as Si_D, and a suboxide transition region between the Si substrate and the bulk SiO₂ layer. The best fit to the observed scattering was obtained with a two monolayer reconstructed substrate Si layer

at the interface, and a suboxide transition layer with an average composition of SiO and approximately 0.25 to 0.5 nm thick [13].

3.1.2 spectroscopic and single wavelength ellipsometry

Spectroscopic ellipsometry studies confirmed the SiO_x regions, but did not include defective Si in the modeling analysis [4,8]. These results compared the dielectric functions obtained from analysis of experimental data with a model that included the dielectric constants of the bulk Si and the bulk SiO₂ as well as a void fraction at the top of the SiO₂ to account for surface roughness effects. The best fit to the data was obtained by adding a 0.75 ± 0.2 nm interfacial transition with an average composition of SiO to the modeled interface structure. The difference between this result, and the interfacial bonding model obtained from the ion scattering experiments was in the number of layers that defined the departure from an abrupt boundary. In particular the inclusion of a defective Si layer in the analysis of the spectroscopic ellipsometry data would have reduced the thickness of the SiO layer, and brought these results and those for ion scattering into closer agreement.

Single wavelength spectroscopic studies using a 632.8 nm He-Ne laser were performed on thermally-grown SiO₂ on Si(111) faces [9]. Figures 10(a) and (b) illustrate the relaxation of bulk strain in the SiO₂ as a function of annealing temperatures. The SiO₂ films were grown by conventional thermal oxidation in dry O₂ at 850°C to a nominal thickness of 125 nm as determined by single wavelength ellipsometry, and were then furnace annealed in flowing Ar for 30 minutes. The data in Fig. 10(a) indicates a decrease in the optical index of refraction, n , with a threshold of about 950°C and a maximum rate of change at approximately 1050°C as determined by numerical differentiation. The data in Fig. 10(b) indicates a complementary increase in film thickness also with a threshold at about 950°C and a maximum rate of change at approximately 1050°C as determined by numerical differentiation. These changes have been attributed in Ref. 8 to relaxation of intrinsic growth stress. As the stress is relieved in the growth direction, the film thickness increases, and the density of the SiO₂ decreases leading to reductions in the index of refraction that track linearly as expected with the increased physical thickness as shown in Fig. 11.

3.1.3 synchrotron x-ray photoelectron spectroscopy

Interfacial suboxide layers have also been studied by synchrotron x-ray photoelectron spectroscopy [6,15]. The study of Keister et al. was the first to systematically study the changes in the interface bonding as a function of annealing temperature [6], and in particular to determine the temperature-dependent changes in relative and absolute concentrations of the specific interfacial local bonding groups: Si bonded to one oxygen, Si¹⁺, to two oxygen atoms, Si²⁺, and to three oxygen atoms, Si³⁺. These concentrations have been converted to an effective interfacial transition layer width in Ref. 16, which after annealing to 900°C in an Ar ambient was equivalent to ~0.4 nm of SiO in good agreement with the values obtained from the ion scattering and

ellipsometry results, respectively of Refs. 13, and 5, 8 and 9.

3.1.4 optical second harmonic generation

A combination of optical second harmonic generation (SHG), single wavelength ellipsometry and capacitance-voltage, C-V measurements identified respectively two different transition temperatures, one for Si-SiO₂ interface relaxation at ~900°C, and one for intrinsic growth stress relaxation at ~1050°C [10]. As shown in Fig. 12, the 900°C relaxation was identified through changes in relative phase in the interference between contributions of terrace and step atoms on vicinal wafers. The relaxation at ~1050°C was identified in Ref. 5, and additionally in Fig. 13 through reductions in the density of interfacial traps, d_{it} , which have previously been correlated with reductions in compressive intrinsic stress in the thermally grown SiO₂ gate oxides [17]. In Ref. 17, the concentrations of d_{it} were demonstrated to scale directly with the total stress in the oxide, including the stress due to differences in the linear coefficients of expansion between Si and SiO₂. Figure 14 contains a plot of the SHG phase angle change as a function of the change in physical film thickness due to relaxation of bulk strain. The most significant changes in the phase angle occur in a temperature regime (see Fig. 10(b)) in which there is only minimal relaxation of bulk strain, whereas the changes in phase angle are minimal in the temperature regime of 950 to 1050°C in which the thickness changes are greatest. The plot in Fig. 14 then clearly illustrates that there are two separate and distinct relaxation processes. The first is due to rearrangements in atomic bonding in the suboxide transition region as revealed in the synchrotron XPS studies of Ref. 2, and the second is due to relief of intrinsic growth stress in the SiO₂ film. These relaxations are now addressed in more detail in the next section of this article.

3. 2 Physical Mechanisms for Interface Relaxation

Lucovsky and Phillips and coworkers applied the concepts of constraint theory developed to explain glass formation in chalcogenide and oxide glasses, to Si-dielectric interfaces [18,19], providing important insights to the physical mechanisms underlying i) the formation of interfacial transition regions, and ii) defect formation and defect relaxation at these interfaces. This approach builds on the studies of Boolchand and coworkers on the nature of the glass transition, and the compositional dependence of transitions in alloy regimes in a glass forming chemical system, e.g., a-Se_{1-x}Ge_x. There are two transitions that are associated with a change from compliant or under-constrained bonding in a-Se, to rigid or over-constrained bonding in an alloy with 33% Ge that span a self organized region that is strain-free. [14]. Lucovsky, Phillips and coworkers pointed out that Si-SiO₂ and Si-Si₃N₄ interfaces were hetero-structures in which in which the substrate Si was rigid or over constrained with the number of bonds/atom equaling exactly four, and the number of valence bonding constraints per atom being greater than the network dimensionality of three. The two dielectrics, SiO₂ and Si₃N₄, have different numbers of bond/atom, and valence bonding constraints per atom, spanning a range from i) an ideal non-crystalline solid for SiO₂ in which the

number of bonding constraints per atom is the same as the network dimensionality, three, to iii) an over-constrained or rigid Si_3N_4 dielectric in which the number of bonding constraints per atom is substantially greater than three. In this paper we apply for the first time constraint theory combined with macroscopic strain, both intrinsic and thermally-generated, to describe interfacial relaxations, and the susceptibility of these interfaces to defect formation under electrical bias.

Differences of more than 25 % between the Si-Si interatomic distances in Si (0.235 nm) and SiO_2 (~0.305 nm) result in intrinsic interfacial strain, tensile in the Si, and compressive in SiO_2 [20]. In addition, differences in linear coefficients of expansion between Si and SiO_2 , also result in an additive contribution of thermally-induced strain after high temperature processing steps.

The combination of bonding constraint differences at the Si-dielectric interfaces, intrinsic bond-length strain, and thermally-induced strain result in multi-component interfacial transitions region as pictured in Fig. 15. After a thermal anneal at 900°C, there is i) a region of strained or defective Si in tensile stress in the Si substrate, ii) a self-organized, strain free transition region with suboxide bonding, and iii) a region in which there is a compressive stain gradient in the stoichiometric dielectric (SiO_2 , Si_3N_4 , or a Si oxynitride alloy). The strain free region represents a balance between intrinsic and thermally induced tensile stress and bond-strain induced compressive stress. Many of the empirically defined metrics for device scaling are determined by this multi-component interfacial region including the universal mobility curves, and the U-shaped variation of d_{it} with energy in the forbidden gap.

3.4 Interface Integrity

Boolchand and coworkers have shown that glasses outside of a narrow compositional *window* in which self-organized, strain free glasses exist, *age irreversibly*, whereas, glasses inside the window, do not age at all [21]. An example of aging is a time dependent change in the glass transition temperature. In this paper, an analogy is drawn between *aging* in glasses, and current or bias voltages stress induced defect generation at Si-dielectric interfaces, either during device operation on a scale of years, or during accelerated stress testing on a scale of hundreds to thousands of seconds. Applying the glass results to the integrity issues is consistent with stress bias/current induced defects being generated in the strained Si region of the substrate, or in the bulk of the dielectric, *but not* in the interfacial SiO_x strain-free region.

In particular, increases in the densities of interface traps which reduce the transconductance through a shallow trap controlled mobility in the channel region, and stretch out the C-V characteristic producing increases in the threshold voltage are associated with defect formation in the strained substrate Si in intimate contact with the SiO_x region, whereas soft and hard break down events take place in the bulk of the dielectric film. These two regions are not strain free either on a bonding scale, or a

macroscopic strain field scale and hence contain strained bonding arrangements that serve as precursor sites for defect formation. However, even though the SiO_x region is not optimized with respect to bonding constraints per atom, there is a relief of this bond strain induced compressive stress and well stress transferred from the SiO_2 layer, by macroscopic tensile stress associated with bond length induced strain of the Si substrate. This cancellation of strain limits the density of precursor sites for defect formation. This cancellation implies a critical thickness to this region, and suggests that if this thickness is exceeded, then the region could be a source of defects and defect precursors. This is indeed the case, and is discussed below.

The application of these ideas to high-k dielectrics is now briefly discussed, and involves applying bond constraint counting approaches that are applicable to ionic bonding arrangements in silicate glasses, and additionally in transition metal high-k dielectrics and Al_2O_3 [22]. For example the average number of bonds/atom in Al_2O_3 is 3, corresponding to 4.5 bonding constraints per atom. For a 30 atomic percent ZrO_2 Zr silicate alloy, $(\text{ZrO}_2)_x(\text{SiO}_2)_{1-x}$, using the method of Kerner and Phillips [22], this corresponds to an average number of bonds per atom of ~ 2.9 , corresponding to ~ 4.2 bond constraints per atom. These increases in bond strain lead to corresponding increases the effective compress stress in the dielectric films, which must be then compensated by proportional increases in tensile stress in the Si substrate. As reported by Stesmans et al. [23,24], this increases the number of density of dangling bond defects by a factor of 4-6 relative to the Si- SiO_2 interface.

The increase in compressive stress in the Zr silicates alloys, which is also anticipated in Hf silicate alloys, both of which are being considered as replacement dielectrics for SiO_2 in aggressively-scaled Si devices, also leads to hysteresis in C-V, traces through the formation of bulk defects in the Zr or Hf dielectric films. Consistent with experiment, these defect which act as shallow trapping sites can not be compensated by termination with H or D. For example, if the defects are associated with broken Zr(H)-O bonds, then H or D defect passivation approaches will favor OH(D) bond formation rather than Zr(Hf)-H(D) consistent with the strong hydrophilic character of Zr and Hf oxide [25], i.e., the formation Zr(Hf)-OH bonds or dative bonding with H_2O molecules after exposure to ambient water vapor. This is due to large differences in the respective Zr(Hf)-H and O-H bond energies, $<1\text{eV}$ and compared to $>3\text{eV}$.

The results of this section can also be applied to interfaces between compound semiconductors and SiO_2 , as for example GaN- $\text{GaO}_x\text{-SiO}_2$, with $x \sim 1.5$ as discussed in Refs. 22 and 23. The GaO_x layer is formed by a pre-deposition remote plasma assisted oxidation (RPAO), and the SiO_2 film is deposited at 300°C by remote plasma enhanced chemical vapor deposition (RPECVD) [26,28]. Devices with SiO_2 deposited directly onto GaN have significantly higher densities of interfacial traps, d_{it} , even after $800\text{-}900^\circ\text{C}$ post deposition anneals. In situ spectroscopic studies indicate that the GaN substrates oxidizes during the initial stages of the SiO_2 deposition, but that this subcutaneous

process which leads to defective interfaces in Si-SiO₂ interfaces is effectively suppressed if an RPAO step precedes the deposition of the SiO₂ dielectric [29]. As in the case of Si-SiO₂ interfaces, a post RPAO, plasma assisted interface nitridation further reduces d_{it} [27,29]. The results of this study suggest similar interface and film relaxation processes are operative in the processing of these GaN interfaces. However, in this instance instead of the interfacial GaO_x layer being self-organized to reduce only interfacial bond coordinated induced strain and macroscopic strain in due to a mismatch of linear thermal expansion coefficients between SiO₂ and GaN, it must also provide charge exchange to reduce defects to the heterovalent nature of the interface, i.e., the fractional number of electrons available per dangling bond at the GaN(0001) interface [30]. Figure 16 compares defects and defect generation in Si-SiO₂ and GaN-SiO₂ structures.

There are two other pieces of experimental data that support the model for interfacial bonding defects. These both relate to growing suboxide layers thicker than an empirically determined optimum. The results for GaN-GaO_x-SiO₂ are summarized in Fig. 8(a), and those for Si-SiO_x-SiO₂ in Fig. 17(b). Fig. 17(a) displays changes in d_{it} as function of interfacial processing. The 30 second RPAO is optimum, and increasing this to 180 seconds results in thicker interfacial oxide as determined by on-lines AES in Refs. 26 and 27, and leading to an increase in d_{it} . In the context of the model, the increases compressive bonding strain in the interfacial GaO_x layer increases the tensile stress in the GaN substrate and thereby increases d_{it} . Post RPAO nitridation reduces the intrinsic bonding stress mismatch at GaN-GaO_x interface, and since the plasma nitridation process gives a higher nitrogen concentration than the RPAO using N₂O, it is more effective in reducing defects. For the nitridation studies, the RPAO was optimized at 30 seconds. Figure 17(b) shows reliability data for Si-SiO_x-Si oxynitride structures. Increasing the RPAO process to give 0.8 nm of oxide, rather than 0.6 nm, i.e., 3 rather than 2 molecular layers of SiO equivalent, increases interfacial strain, and reduces reliability expressed here as time to dielectric breakdown (TTBD) [31].

3.5. Summary

Studies of Si(111)-SiO₂ interfaces by optical second harmonic generation in Ref. 6-8 were first to identify a strongly temperature dependent interfacial relaxation with an onset of ~900°C. Coupled with determinations of d_{it} from C-V measurements, the results presented in Ref. 6 were the first to differentiate between two distinctively different relaxations at Si-SiO₂ interfaces, one at 900°C associated with interface bonding changes, and a second at ~1050°C associated with relief of intrinsic compressive stress in the SiO₂ film. Complementary studies by synchrotron x-ray photoelectron spectroscopy have established that this relaxation is associated with changes in concentration and composition of suboxide bonding environments in an ultrathin interfacial transition region that is approximately two molecular layers thick, ~0.5 nm. This relaxation occurs at a significantly lower temperature than an approximately 1050°C relaxation of macroscopic compressive strain in the bulk of the

SiO₂ film [17]. This paper has provided important new insights into these two distinct relaxation phenomena. It has demonstrated an analogy between i) the Si-SiO₂ interface in which there is a transition from a rigid substrate to an ideal random covalent network, and ii) compositionally dependent under and over-constrained bonding in glass alloys such as Ge_xSe_{1-x} [14,21]. The interfacial suboxide transition region has been demonstrated to have properties in common with a regime of alloy compositions in which self-organization reduces bond constraint induced strain, thereby stabilizing these compositions against *aging*. This has provided important insights into defect formation at semiconductor dielectric interfaces including Si-SiO₂ as well Si interfaces with alternative high-k dielectrics such as Al₂O₃ and transition metal silicate alloys. The results of this study predict increased defects the interfaces, Si dangling bonds, and interface traps within the strained Si substrate, and precursor sights for soft and hard breakdown with the dielectric.

4. Band offset energies

The properties of *clean* n- and p-type GaN (0001) surfaces and the interface between this surface and SiO₂, Si₃N₄, and HfO₂ have been investigated. The apparatus for these studies is shown in Fig. 18, which shows a multi-chamber UHV system with chambers for sample introduction, plasma processing, and on-line analysis by AES, XPS and UPS. In summary, both n- and p-type Ga-face GaN (0001) surfaces have been cleaned via an 860°C anneal in an ammonia atmosphere, and carbon and oxygen contaminants were reduced to below the detection limits by XPS, (< 1 atomic percent). The N₂ plasma clean discussed above gave similar results as shown in Fig. 3. Thin films of SiO₂, Si₃N₄, or HfO₂ were deposited under conditions which limited the reaction between the plasma generated oxygen and nitrogen species and the underlying GaN surface. After stepwise depositions of Si and Hf, and subsequent oxidations and nitridations, the electronic states were measured with x-ray photoelectron spectroscopy (XPS) and ultraviolet photoemission spectroscopy (UPS). A valence band offset (VBO) of 2.0 ± 0.2 eV with a conduction band offset (CBO) of 3.6 ± 0.2 eV was determined for the GaN/SiO₂ interface. The large band offsets suggest SiO₂ is an excellent candidate for passivation of GaN. For the GaN/Si₃N₄ interface, type II band alignment (the valence band edge of Si₃N₄ was at a higher energy with respect to vacuum, than the valence band edge of GaN) was observed with a VBO of -0.5 ± 0.2 eV with a CBO of 2.4 ± 0.2 eV. While Si₃N₄ should passivate n-type GaN surfaces, it is not suitable for p-type GaN surfaces. A VBO of 0.4 ± 0.2 eV with a CBO of 2.0 ± 0.2 eV was determined for the GaN/HfO₂ interface. An instability was observed in the HfO₂ film, with energy bands shifting ~0.5 eV during a 650 °C densification anneal. The electron affinity measurements via UPS were 3.0, 1.1, 1.8, and 2.9 ± 0.1 eV for GaN, SiO₂, Si₃N₄, and HfO₂ surfaces, respectively. Electron affinity measurements, along with band alignment data, allow a deviation from the electron affinity model due to a change of the interface dipole to be observed. Interface dipoles of 1.7, 1.1 and 1.9 ± 0.2 eV were observed for the GaN/SiO₂, GaN/Si₃N₄, and GaN/HfO₂ interfaces, respectively. The existence of Ga-

O bonding at the heterojunction significantly increases the interface dipole, which raises the dielectric bands in relation to the GaN.

4.1 GaN/SiO₂ interfaces

The band alignment at the SiO₂-GaN interface is important for passivation of high voltage devices and for gate insulator applications. X-ray photoelectron spectroscopy and ultraviolet photoemission spectroscopy have been used to observe the interface electronic states as SiO₂ was deposited on clean GaN (0001) surfaces. Figure 19 displays the oxygen atom 1s XPS spectra after the chemical vapor clean (CVC), an 860°C anneal in an NH₃ atmosphere, and after exposure to an O₂ plasma in the RPECVD chamber, and finally after formation of a SiO₂ layer formed by deposition of Si and subsequent plasma assisted oxidation. As measured by XPS, the as-loaded GaN sample contains ~14 and 8 atomic percent of oxygen and carbon, respectively. The chemical vapor clean (CVC) clean reduces the oxygen and carbon below the XPS detection limits (< 1 atomic percent). The marker for trace (b) indicates the position of the GaO_x, $x < 1.5$ oxide formed on the GaN, and the marker for the trace in (c), the core line energy for oxygen in SiO₂. The core level for plasma oxidized GaN was used to confirm that GaO_x was not formed during the SiO₂ deposition process which consisted of Si depositions followed by plasma oxidation.

The substrates, grown by metallorganic chemical vapor deposition, were n-type (1×10^{17}) and p-type (2×10^{18}) GaN on 6H-SiC (0001) with an AlN (0001) buffer layer. The GaN surfaces were atomically cleaned via an 860°C anneal in an NH₃ atmosphere. For the clean surfaces, n-type GaN showed upward band bending of 0.3 ± 0.1 eV, while the p-type GaN showed downward band bending of 1.3 ± 0.1 eV. These are indicated respectively in Figs. 20 and 21. Also marked on Figs. 20 and 21, at the respective electron affinities for n-type and p-type GaN at 2.9 ± 0.1 eV and 3.2 ± 0.1 eV, respectively. To avoid oxidizing the GaN, layers of Si were deposited on the clean GaN surface via ultrahigh vacuum e-beam deposition, and the Si was oxidized at 300°C by a remote O₂ plasma. The substrates were annealed at 650°C for densification of the SiO₂ films. Surface analysis techniques were performed after each step in the process, and yielded a valence band offset (VBO) of 2.0 ± 0.2 eV and a conduction band offset (CBO) of 3.6 ± 0.2 eV for the GaN-SiO₂ interface for both p- and n-type samples. Interface dipoles of 1.8 eV and 1.5 eV were deduced for the n- and p-type GaN-SiO₂ interfaces, respectively. These results are summarized in Fig. 22, where comparisons are made between the band alignments at Si/SiO₂, SiC/SiO₂ and GaN/SiO₂ interfaces.

4.2 GaN/Si₃N₄ interfaces

X-ray photoelectron spectroscopy (XPS) and UV photoelectron spectroscopy (UPS) were used to measure the electronic states as Si₃N₄ was deposited on clean GaN (0001) surfaces (see Fig. 23). The n-type (2×10^{18}) and p-type (1×10^{17}) GaN surfaces were atomically cleaned in NH₃ at 860°C, and the n- and p-type surfaces showed upward band bending of $\sim 0.2 \pm 0.1$ eV and downward band bending of $1.1 \pm$

0.1 eV, respectively, both with an electron affinity of 3.1 ± 0.1 eV. Layers of Si (~0.2 nm) were deposited on the clean GaN and nitrided using an electron cyclotron resonance (ECR) N_2 plasma at 300 °C and subsequently annealed at 650°C for densification into a Si_3N_4 film. Surface analysis was performed after each step in the process, and yielded a valence band offset (VBO) of 0.5 ± 0.1 eV. Both interfaces exhibited type II band alignment where the valence band maximum of the GaN lies below that of Si_3N_4 valence band. The deduced conduction band offset (CBO) is found to be 2.4 ± 0.1 eV, and a change of the interface dipole of 1.1 ± 0.1 eV was observed for the Si_3N_4 /GaN interface formation.

Figures 24 and 25 display energy level alignments in-situ cleaned n-type and p-type GaN surfaces, and their respective interfaces interface between n-type and p-type GaN, and Si_3N_4 . Figure 26 compares the band alignments of Si/ Si_3N_4 and GaN/ Si_3N_4 interfaces.

4.3 GaN/HfO₂ interfaces

The XPS and UPS spectra were obtained after each process step in a sequence of experiments to follow the shifts of the XPS peaks and the evolution of the valence band spectra. The spectra were measured to track the peak shifts and discern the band bending and band offsets after each of the following steps: a 0.4 nm Hf deposition, O_2 plasma at 300°C, 0.4 nm Hf (0.8 nm total Hf) and O_2 plasma at 300 °C, 650 °C anneal for 15 minutes, a final 0.4 nm Hf deposition (1.2 nm Hf total) and O_2 plasma at 300 °C, and a 15 minute 650 °C final anneal. The final thickness of the HfO₂ film was calculated to be ~2.0 nm based on bulk densities, and the thickness as determined experimentally was found to be ~2.0 nm by comparing the Si 2p XPS core level intensities after the CVC and final HfO₂ deposition steps.

Figure 27 displays the evolution of the oxygen 1s core level. As measured by XPS, the as-loaded GaN sample contains ~14 and 8 atomic percent of oxygen and carbon, respectively. The chemical vapor clean (CVC) clean reduces the oxygen and carbon below the XPS detection limits (< 1 atomic percent). After deposition of 0.4 nm Hf and the O_2 plasma, the initial peak position was observed at 529.9 ± 0.1 eV. Through the course of the experiment, the peak shifted to 530.7 eV, a difference of 0.8 ± 0.1 eV.

The oxide quality is an important issue because it affects the bandgap of the material. Careful comparisons were made of the HfO₂ grown on the GaN surface to HfO₂ grown on silicon. The difference in energy between the O 1s and Hf 4f core levels was found to be 511.6 eV in the oxide grown on GaN which indicates that the HfO₂ film grown on GaN is the same as the HfO₂ grown on Si.

The spectral peak positions and the full width-half maximum (FWHM) of the Ga $3p_{3/2}$, Hf 4f, O 1s, Ga 3d, and N 1s that there is no significant reaction at the GaN-HfO₂ interface during the HfO₂ growth process.

The band alignment of an HfO₂ layer on $1 \times 10^{17} \text{ cm}^{-3}$ n-type GaN has been investigated. Annealing in ammonia at 860°C provided atomically clean, stoichiometric GaN surfaces with $0.3 \pm 0.1 \text{ eV}$ upward band bending. The electron affinities for the clean n-type GaN and HfO₂ were measured to be 3.0 and 2.9 eV, respectively. After careful formation of the GaN-HfO₂ interface, upward band bending of 0.4 and $0.9 \pm 0.1 \text{ eV}$ was found for the as grown and annealed interface, respectively. A valence band offset of $0.1 \pm 0.1 \text{ eV}$ was obtained for the as grown interface, with a conduction band offset of $2.5 \pm 0.1 \text{ eV}$ (assuming $E_{g \text{ HfO}_2} = 5.8 \text{ eV}$). For the annealed interface, a valence band offset of $0.4 \pm 0.1 \text{ eV}$ was obtained, while the conduction band offset was determined to be $2.0 \pm 0.1 \text{ eV}$. This result suggests the thermal stability of the hafnium oxide film greatly affects the electronic properties at the GaN-HfO₂ interface. The interface dipole deduced from comparison with the electron affinity model was 2.0 and 1.9 eV before and after annealing, respectively, for the GaN-HfO₂ interface. The charge neutrality model does not reliably predict the band alignment of the GaN-HfO₂ interface. These results suggest that HfO₂ may be appropriate for passivation of n-type surfaces, but should not passivate p-type surfaces.

Figures 248 and 29 display energy level alignments in-situ cleaned n-type and p-type GaN surfaces, and their respective interfaces interface between n-type and p-type GaN, and HfO₂.

5. Summary

This report summarizes the three research accomplishments: i) the development of a remote plasma processing sequence that yields device quality interfaces between GaN and SiO₂, ii) the development of a new understanding of semiconductor dielectric interfaces in general which identifies the importance of interface suboxide transition regions, and iii) the determination of band alignments at interfaces between n-type and p-type GaN and SiO₂, Si₃N₄ and HfO₂ dielectrics.

If funds become available, it is strongly recommended that the program be extended to include: i) remote plasma processing for GaN interfaces with Si₃N₄, and alternative high-k dielectrics, including HfO₂, Hf silicate and aluminate alloys, and other new materials that are currently under study, and ii) that interface studies should be extended to (Al,Ga)N and (In,Ga)N substrates as well.

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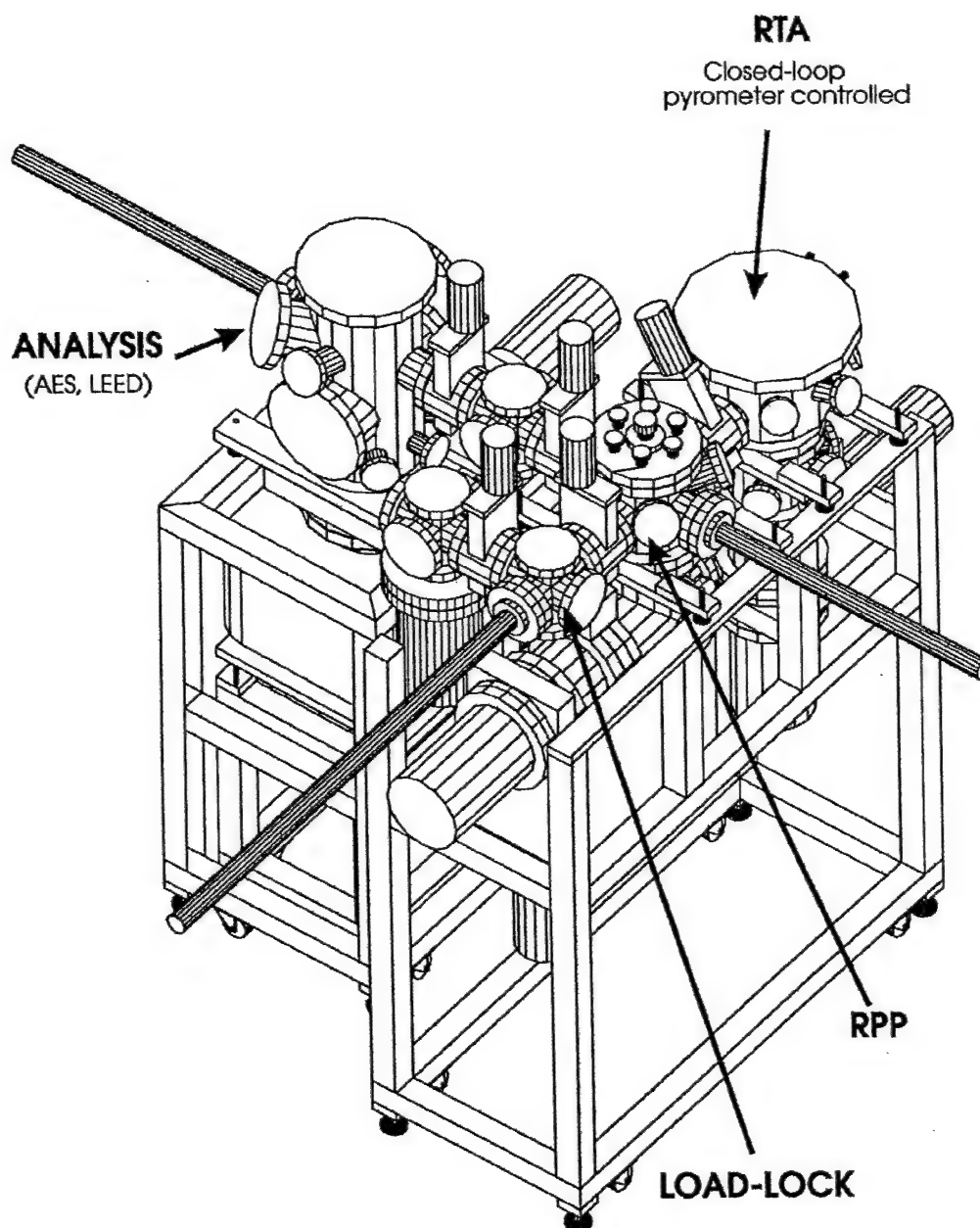


Figure 1. Schematic of multi-chamber integrated processing system that includes the following chambers; i) load lock substrate introduction, ii) remote plasma processing (RPP), iii) on line analysis, Auger electron spectroscopy (AES), and back view low energy electron diffraction (LEED), and iv) rapid thermal annealing (RTA).

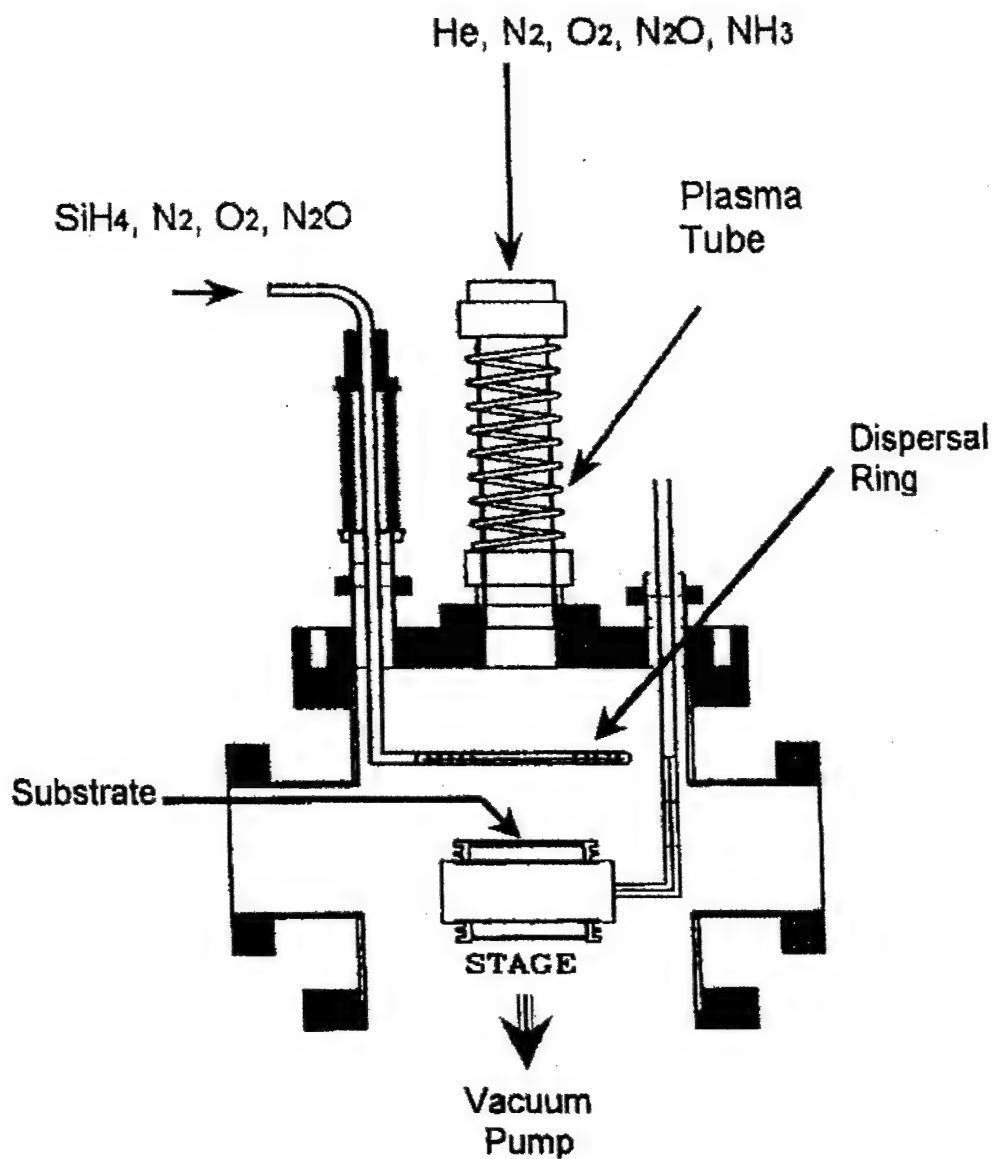


Figure 2. Cross sectional view of remote plasma processing chamber, including substrate heater, downstream injection showerhead dispersal ring, plasma excitation region for upstream injection, and port for coupling to vacuum pumping system.

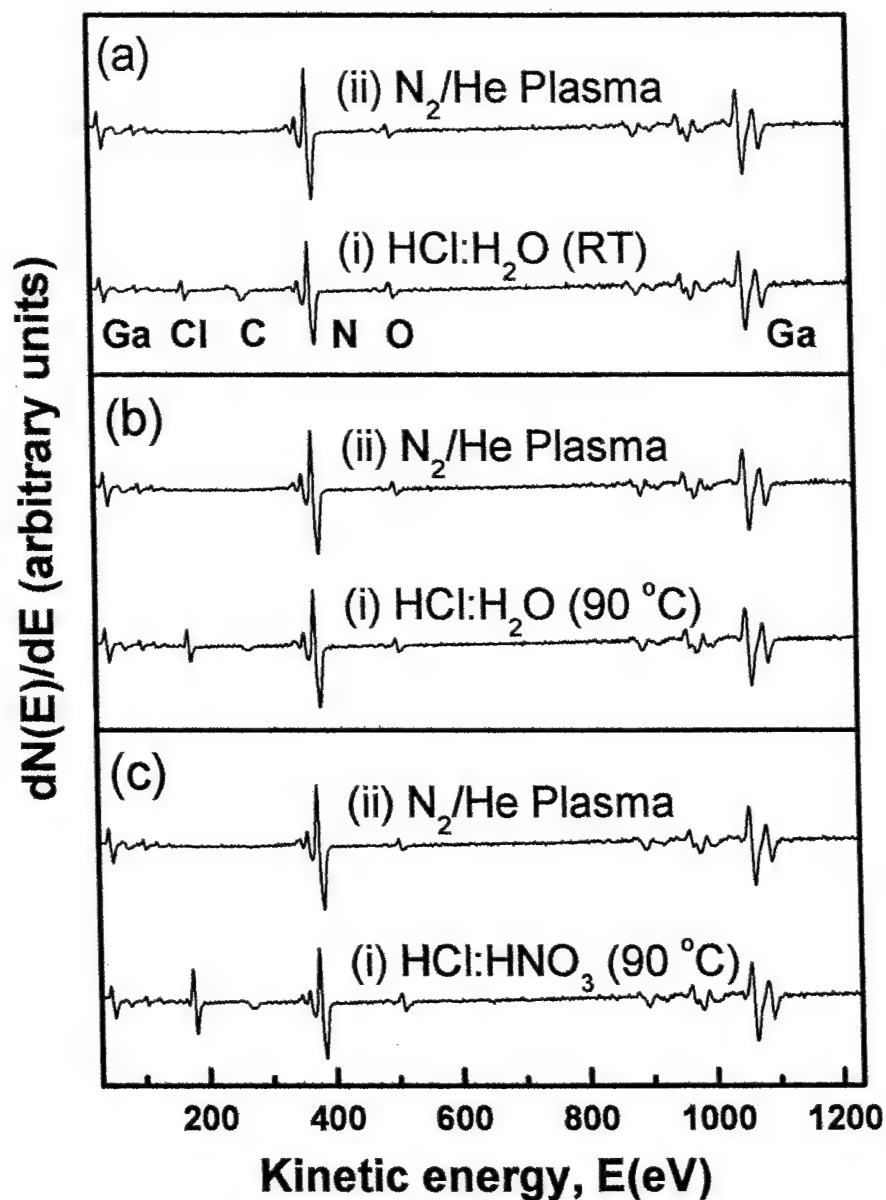
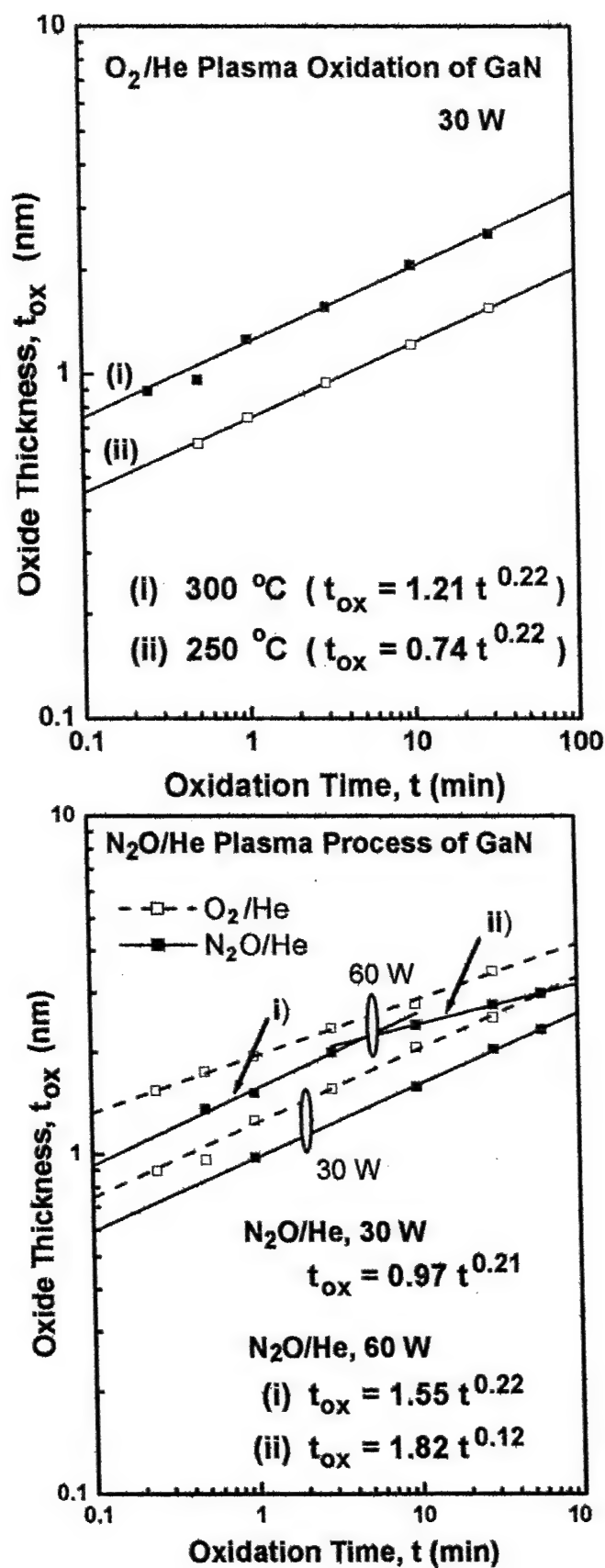


Figure 3. Differential AES spectra of GaN surface after etching in (a) 1:1 $HCl:H_2O$ (RT), (b) 1:1 $HCl:H_2O$ (90 °C) and (c) 3:1 $HCl:HNO_3$ (90 °C). After *in situ* N_2/He plasma treatment at 0.02 Torr, C and Cl were reduced below AES measurement limit of detection and O KLL/N KLL reduce to ~ 0.06 regardless of varied wet chemical treatments.

Figure 4. Oxidation kinetics for RPAO process. (a) O_2 source gas, and (b) N_2O source gas.



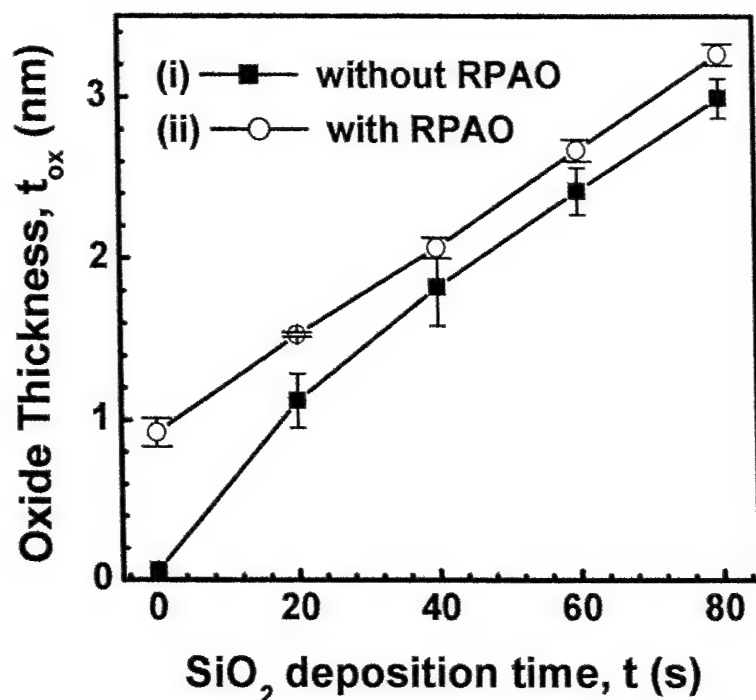


Figure 5. Oxide thickness versus SiO₂ deposition with and without the RPAO step, illustrating ~ 0.3 nm of subcutaneous oxidation during deposition without RPAO step.

Figure 6. C-V traces after using the RPAO (O₂) process after the wet clean. This reduces the frequency dependent spread between the traces by more than a factor of five. The top trace (a) is for a 30 s oxidation, and the bottom trace (b) for a 180 s oxidation.

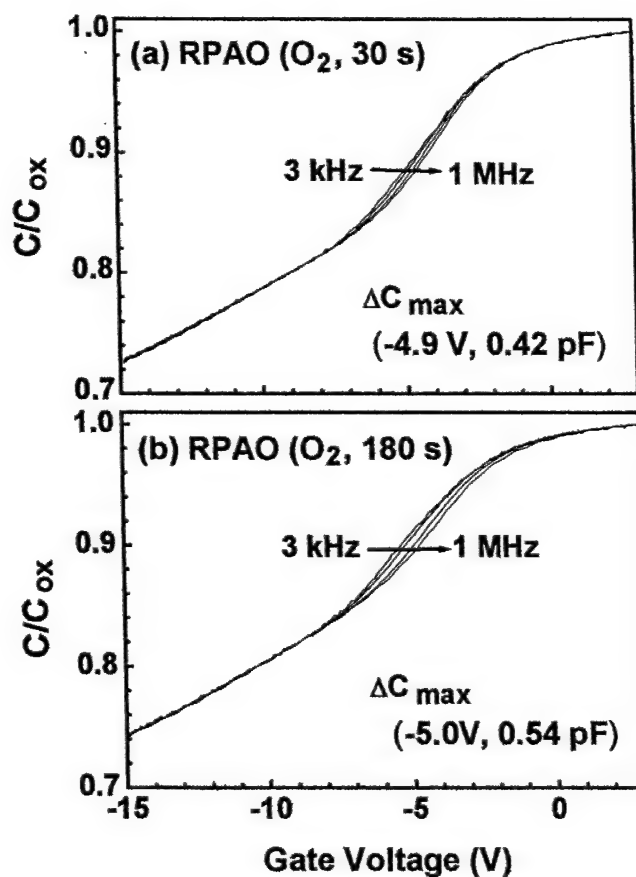


Figure 7. C-V traces after using the RPAO process after the wet clean. Trace (a) is for a process in which N_2O has been substituted for O_2 , and trace (b) is for a process in O_2 is used for the RPAO, but this is followed by an RPAO step.

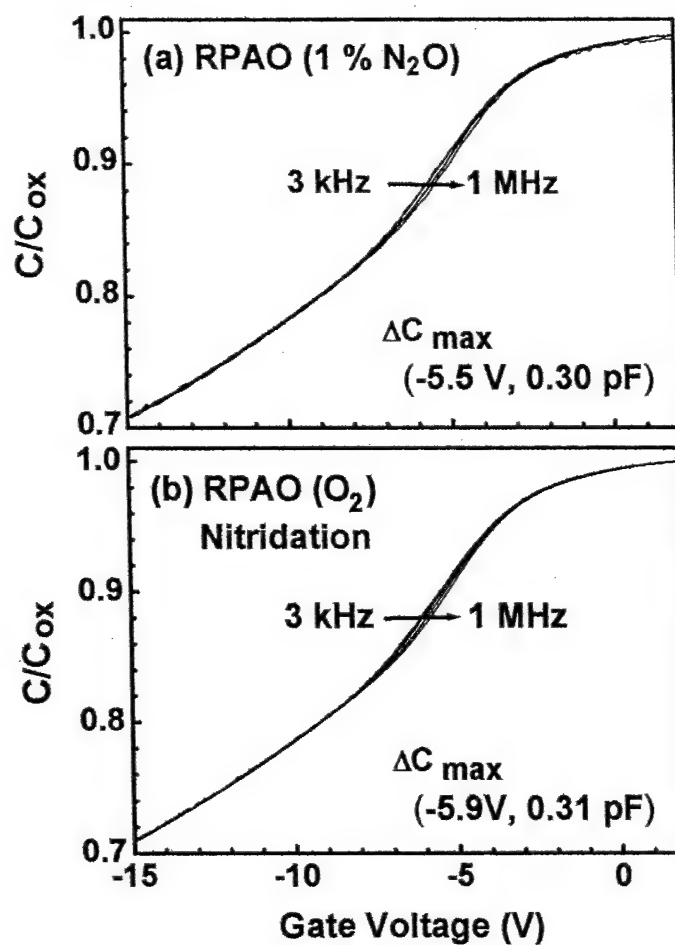


Figure 8. Comparison of interface defects for O_2 , N_2O and O_2 /nitridation pre-deposition processes

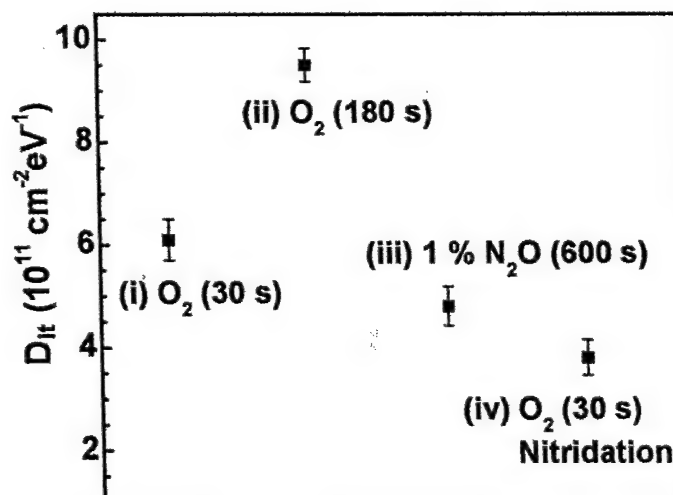


Figure 9(a) Comparison between measured and calculated C-V. The highlighted separation between measured and calculated C-V trace indicates deep depletion effect.

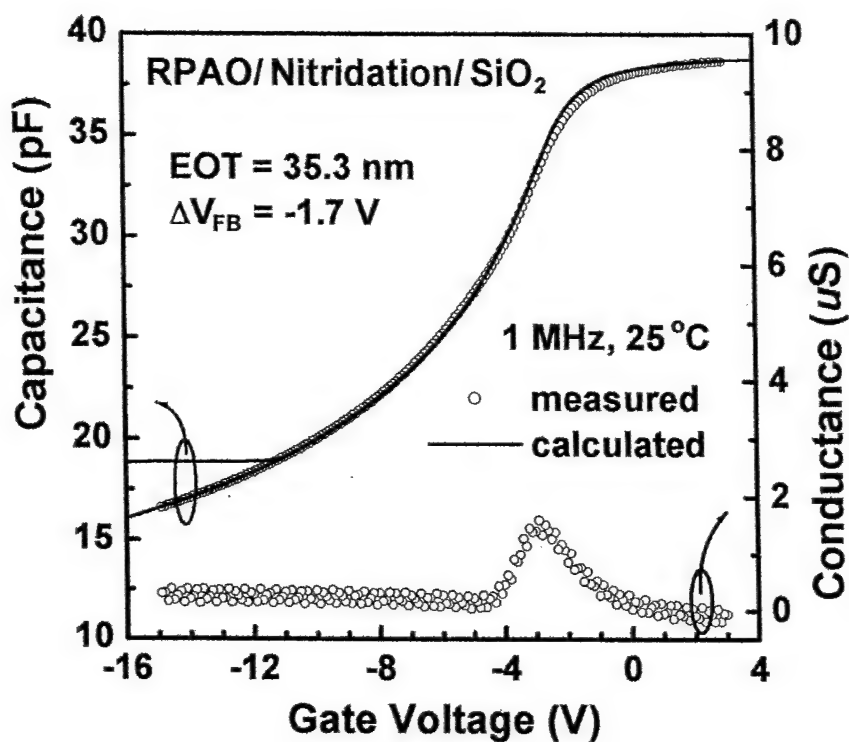
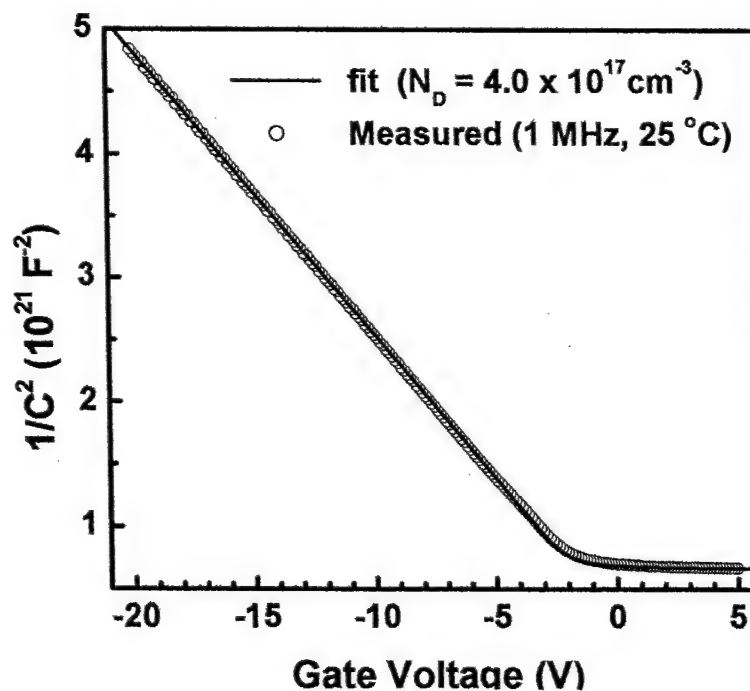


Figure 9(b) Plot of $1/C^2$ versus gate voltage is consistent with depletion width determined by donor density in the GaN substrate.



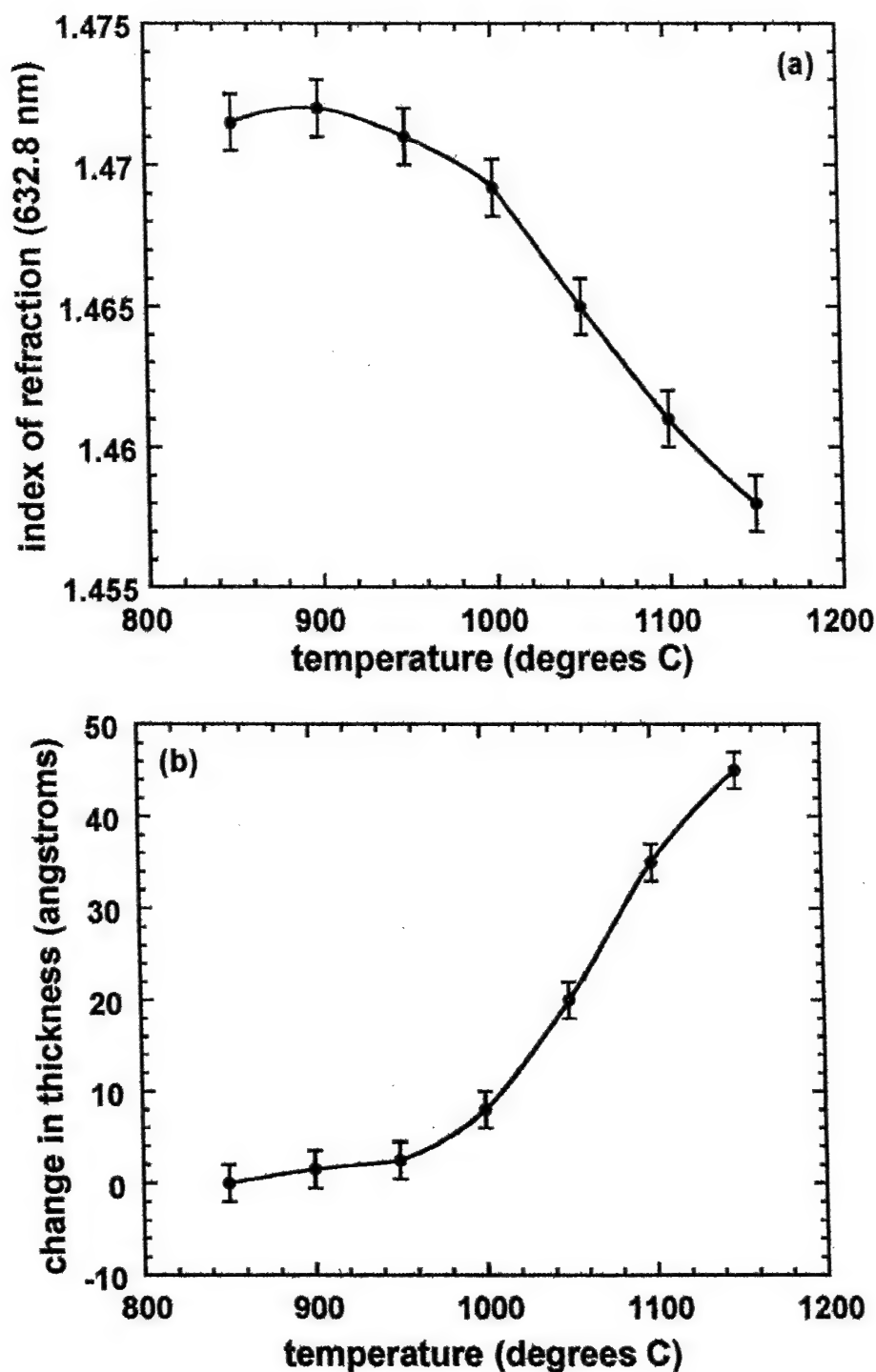


Figure 10. Changes in the properties of SiO₂ films grown on Si(111) by conventional thermal oxidation in dry O₂ at 850°C, and subsequently annealed in flowing Ar for 30 minutes, as determined by single wavelength ellipsometry. (a). The optical index of refraction at 632.8 nm as a function of processing temperature. (b) Changes in the film thickness as a function of processing temperature. The solid lines are interpolations that establish the trends in the data points.

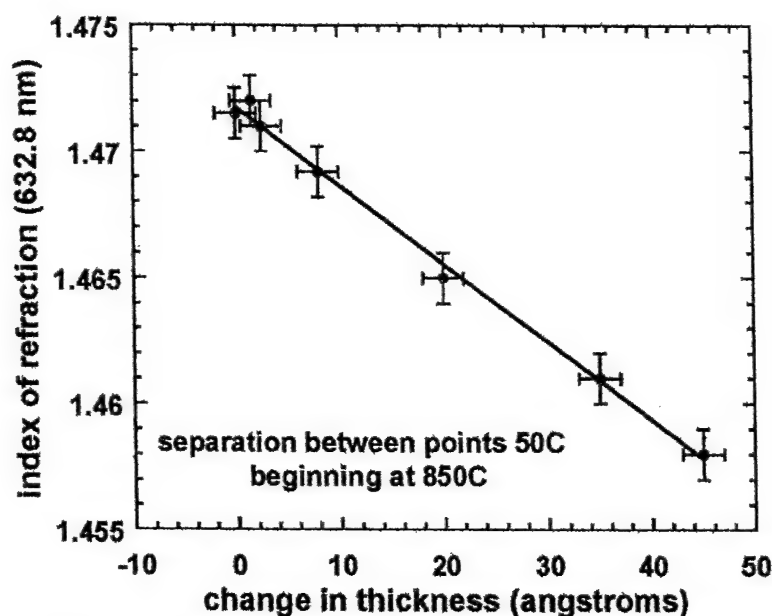


Figure 11. The optical index of refraction at 632.8 nm as a function of changes in the film thickness at a given processing as extracted from the temperature dependent data in Figs. 1(a) and (b). The solid line is an interpolation that establishes the trend in the data points.

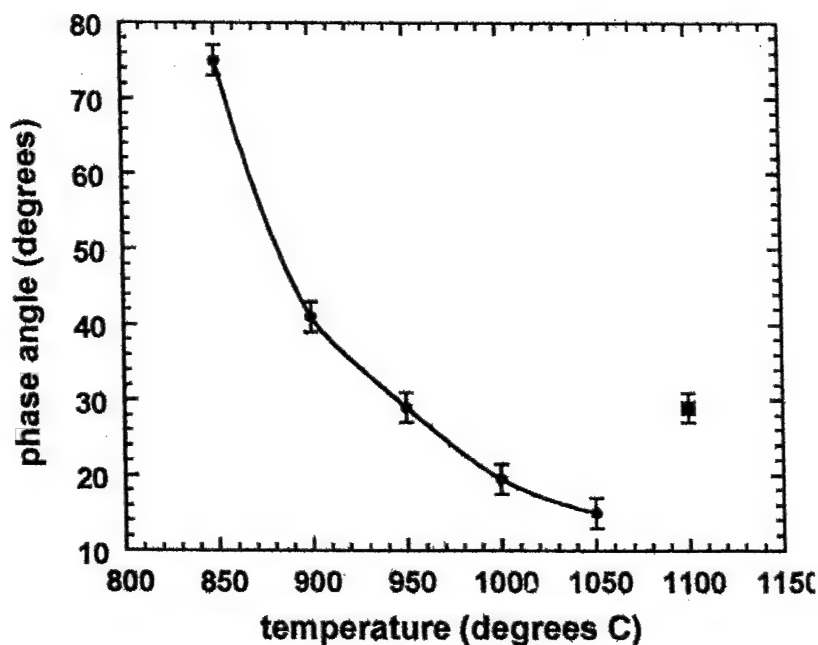


Figure 12. Phase angle difference between terrace and step edge contributions to the optical SHG signal from vicinal Si(111) wafers off cut 5 degrees in the 112bar direction. The point at 1100C does not fall on the trend line and occurs at temperature at which interface decomposition associated with the evolution of gaseous SiO is known to occur. The solid line is shows the trend in the data.

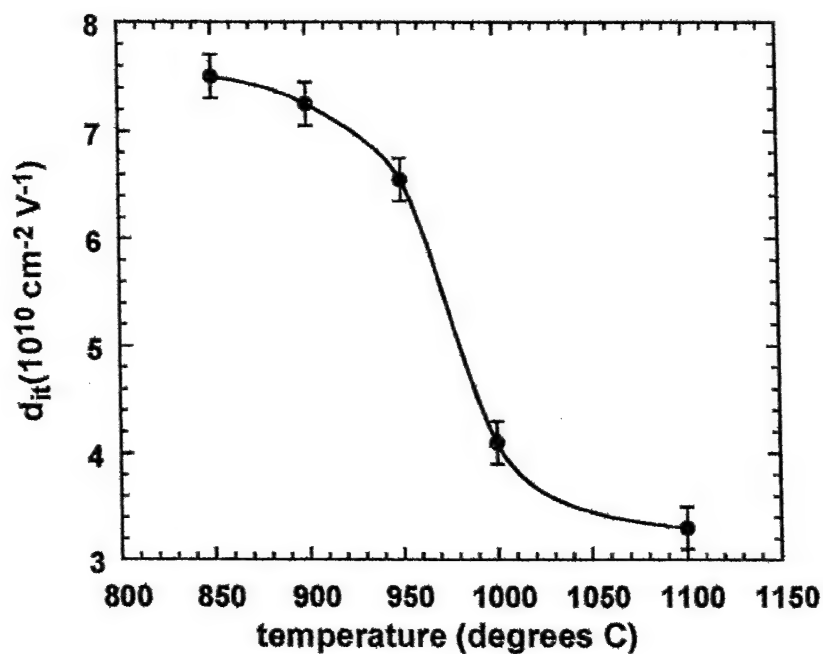


Figure 13. Values of mid-gap densities of interface traps, d_{it} , extracted from C-V measurements on Si(111) metal-oxide-semiconductor structures as function of processing temperature. The solid line is an interpolation that establishes the trend in the data points.

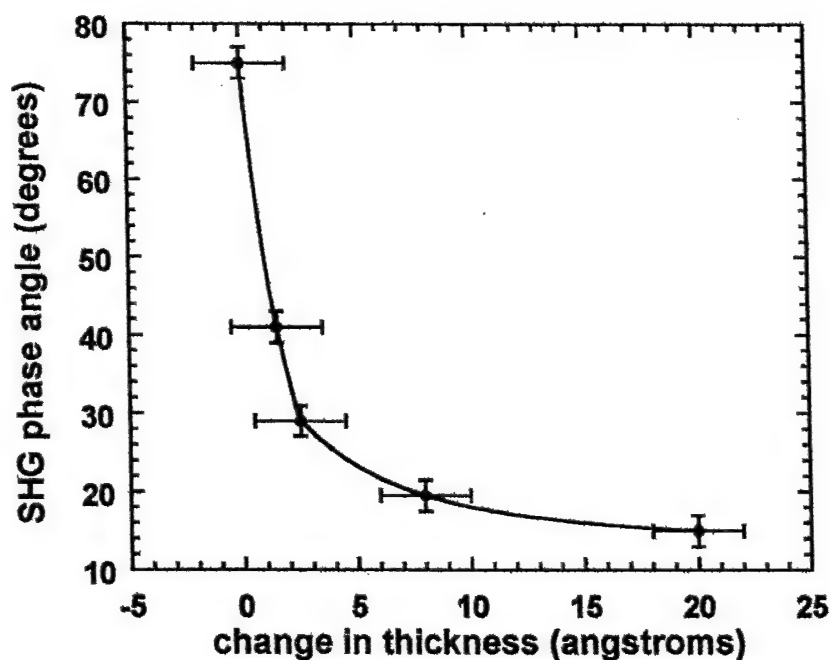


Fig. 14. SHG phase angle versus change in film thickness for Si-SiO₂ structures processed at the same temperatures. The solid line is an interpolation that establishes the trend in the data points.

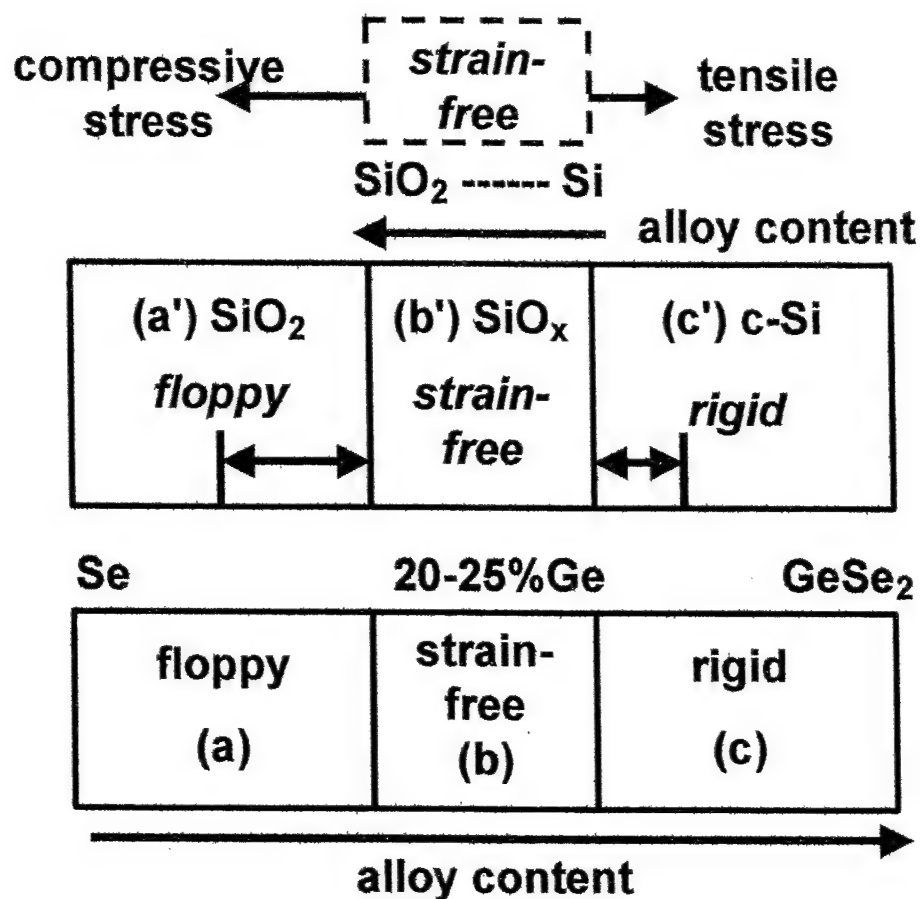


Figure 15. Schematic representation of stress in floppy, self-organized and rigid regions of an SiO_2 - SiO_x - Si structure, and the corresponding regions of the non-crystalline $\text{Ge}_x\text{Se}_{1-x}$ alloy system in the range from Se to GeSe_2 ($x = 0.333$).

<i>Si substrate</i>	<i>strained Si</i>	<i>strain-free SiO_x</i>	<i>compressively-stressed SiO₂</i>	<i>strain-free SiO₂</i>
defects, and stress-induced defects	$D_{it} + \Delta D_{it}$ charge injection	Q_f , fixed charge	soft and hard breakdown precursors	
<i>GaN substrate</i>	<i>strained GaN</i>	<i>strain-free GaO_x</i>	<i>compressively-stressed SiO₂</i>	<i>strain-free SiO₂</i>

Figure 16. Interfacial defects, d_{it} , fixed charge, Q_f , and charge injection for hysteresis, and stress induced defect formation, Δd_{it} and soft and hard breakdown precursors, for Si-SiO_2 and GaN-SiO_2 interfaces.

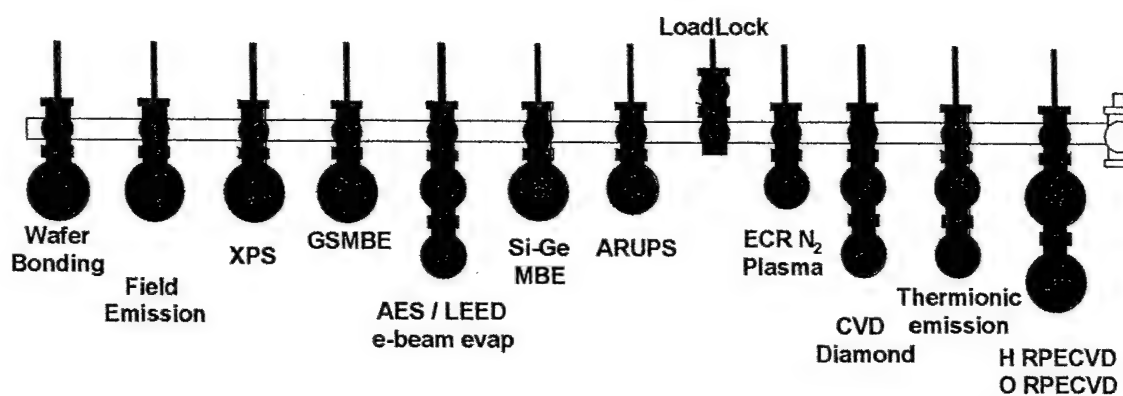


Figure 18. UHV- compatible multi-chamber processing/analysis systems used for studies of band offset energies between GaN and SiO₂, Si₃N₄ and HfO₂.

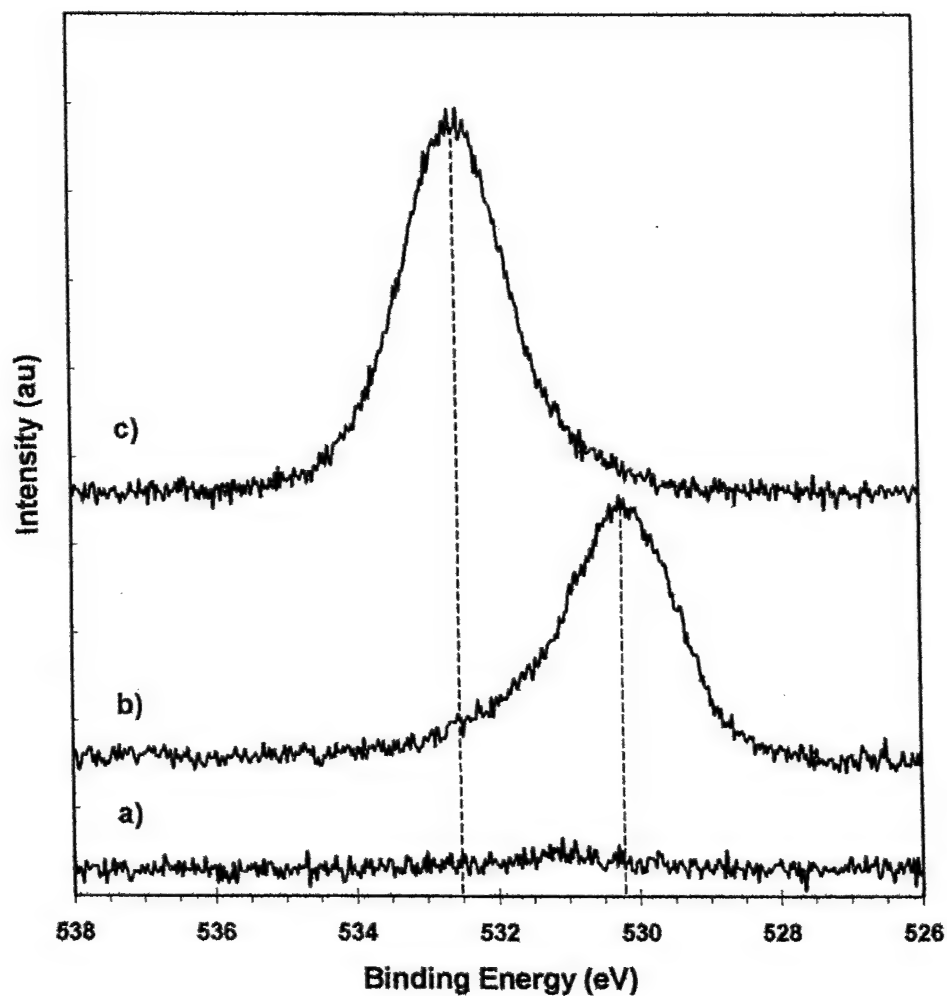


Figure 19. Oxygen 1s XPS spectra for: a) CVC Clean p-GaN, b) O₂ plasma, and c) the final SiO₂ surface. Dashed lines indicate the peak positions for the oxidized GaN, as well as the final SiO₂ surface.

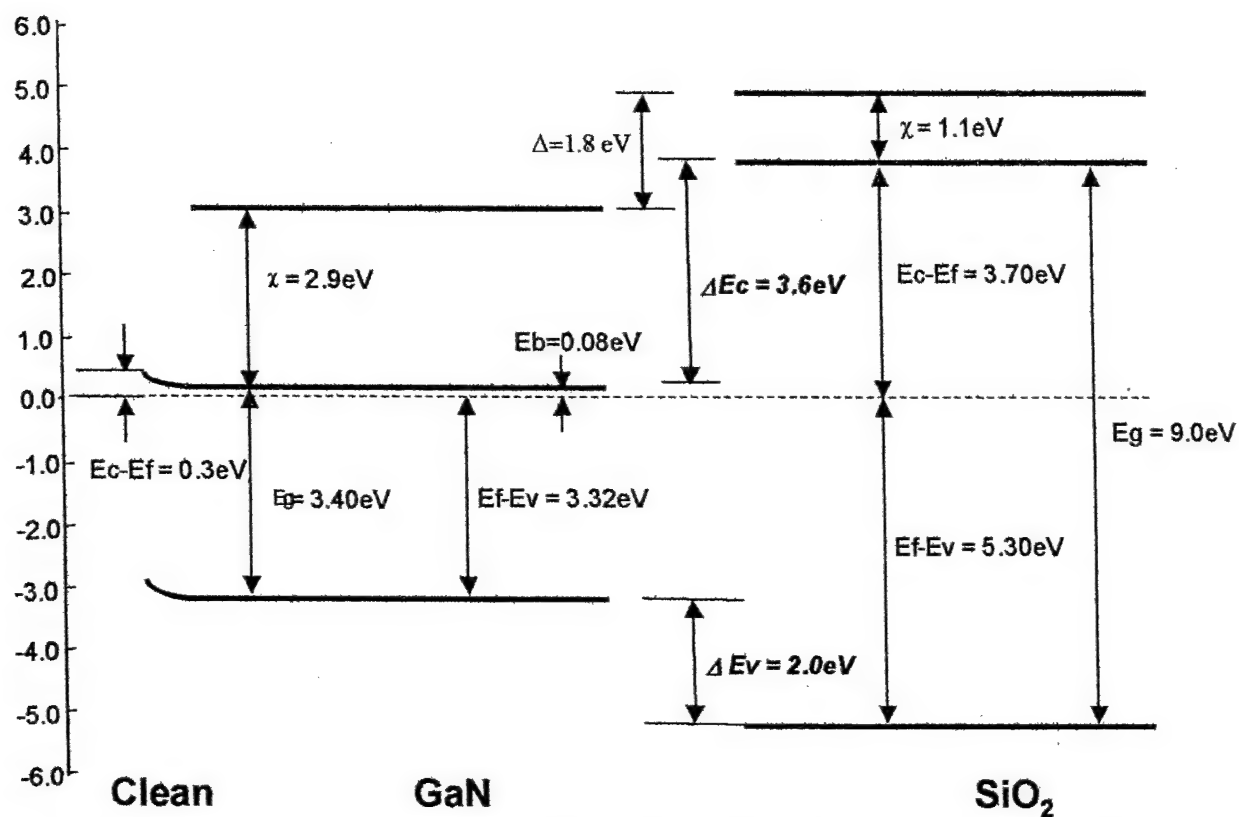


Figure 20. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and SiO₂. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.

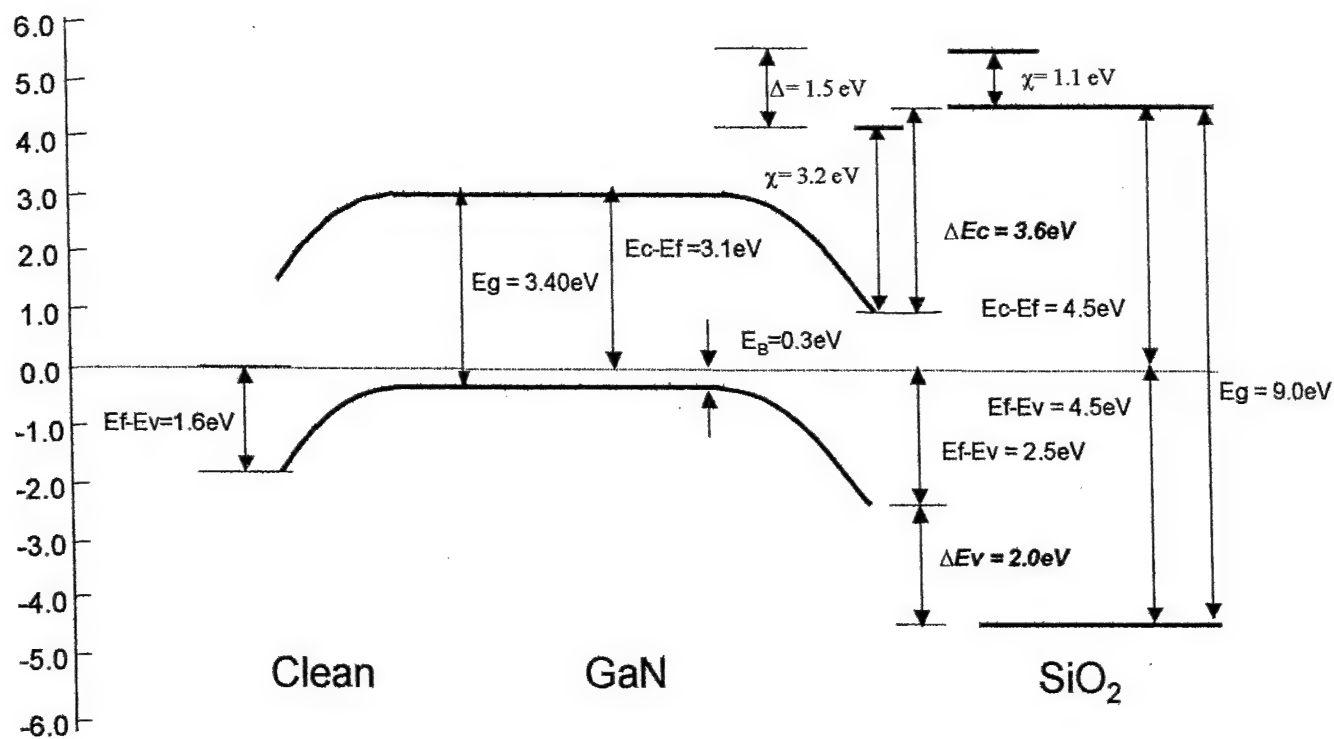


Figure 21. Deduced bands for the clean p-type GaN surface (left) and the interface between p-type GaN and SiO₂. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.

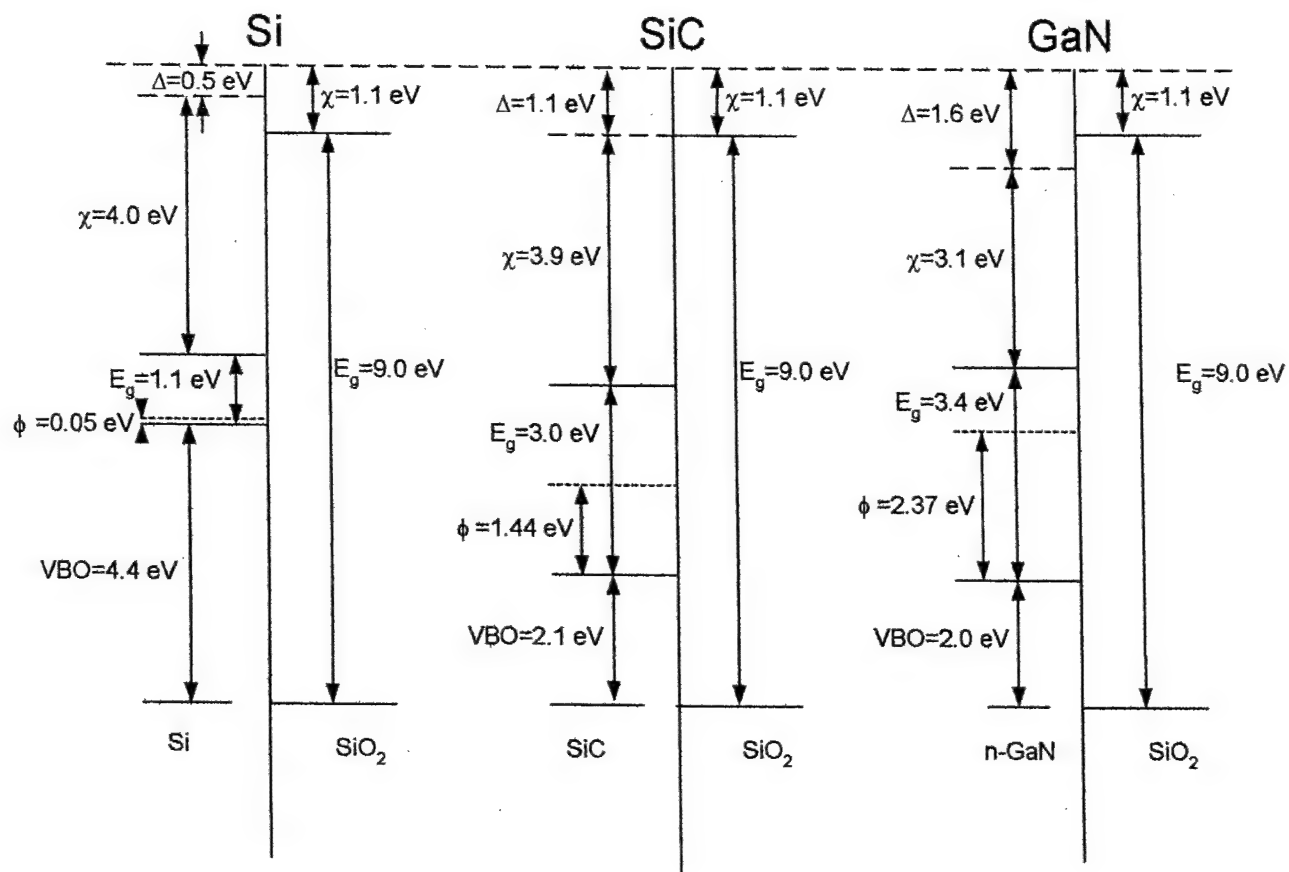


Figure 22. Band alignment of Si/SiO₂, SiC/SiO₂, and GaN/SiO₂ interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the SiO₂ surface, which is common in all three interfaces. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap. The VBO are determined from the measurements.

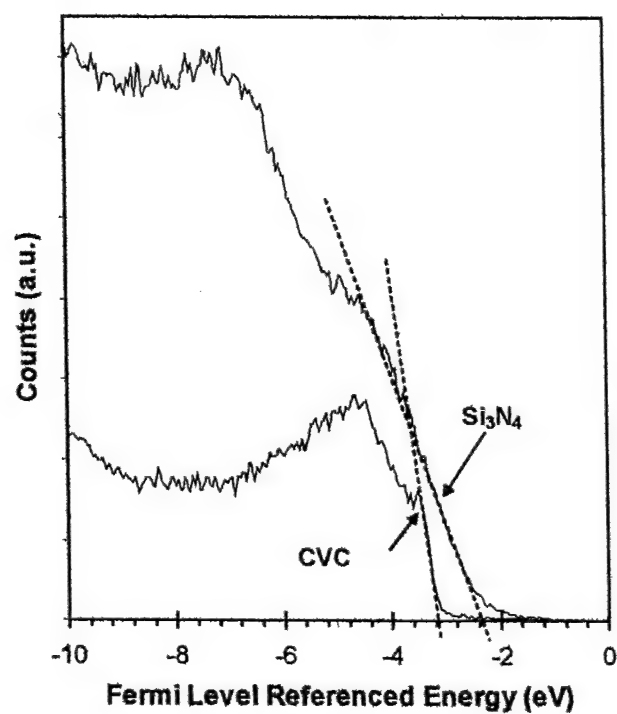


Figure 23. UPS spectra of the Valence Band turn-on of clean GaN and the Si₃N₄ final surface.

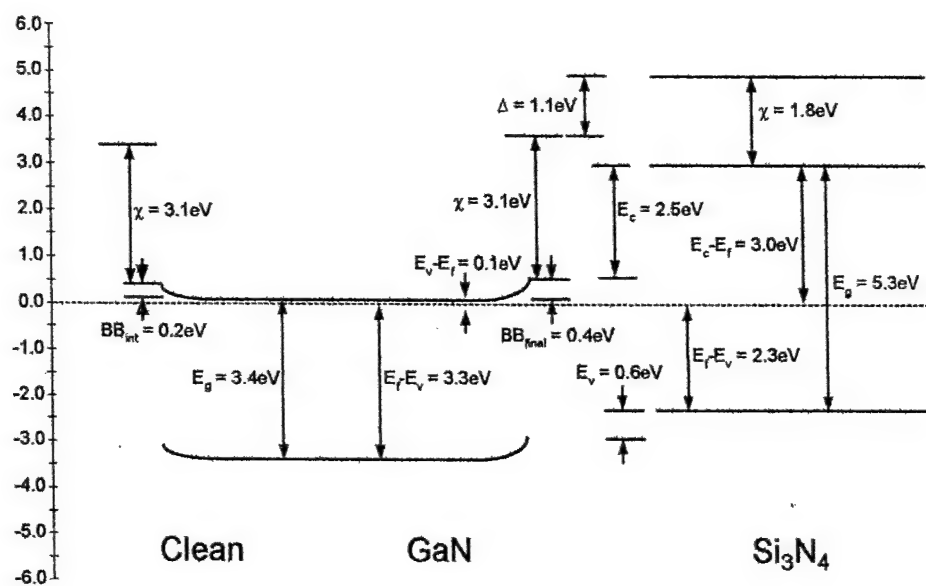


Figure 24. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and Si₃N₄. The valence band offset, E_v , conduction band offset, E_c , band bending, and interface dipole, Δ , are represented.

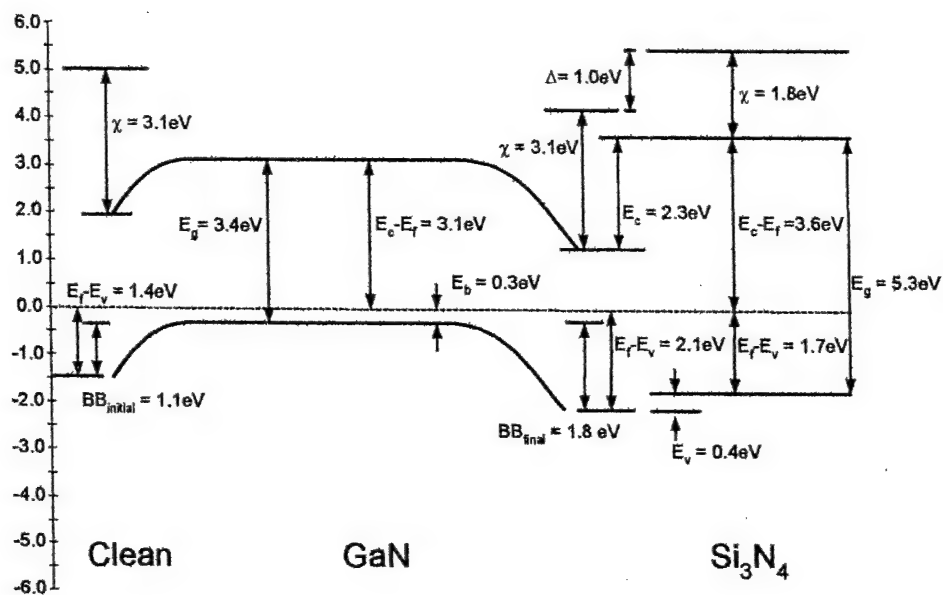


Figure 25. Deduced bands for the clean p-type GaN surface (left) and the interface between p-type GaN and Si₃N₄. The valence band offset, E_v , conduction band offset, E_c , band bending, and interface dipole, Δ , are represented.

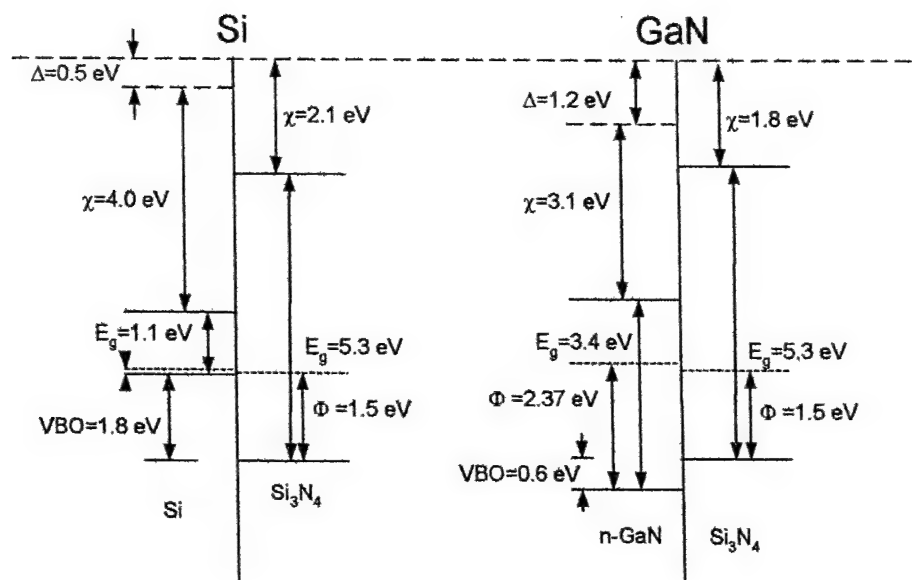


Figure 26. Band alignment of Si/Si₃N₄ and GaN/Si₃N₄ interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the Si₃N₄ surface, which is common in both interfaces. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap. The VBO are determined from the measurements.

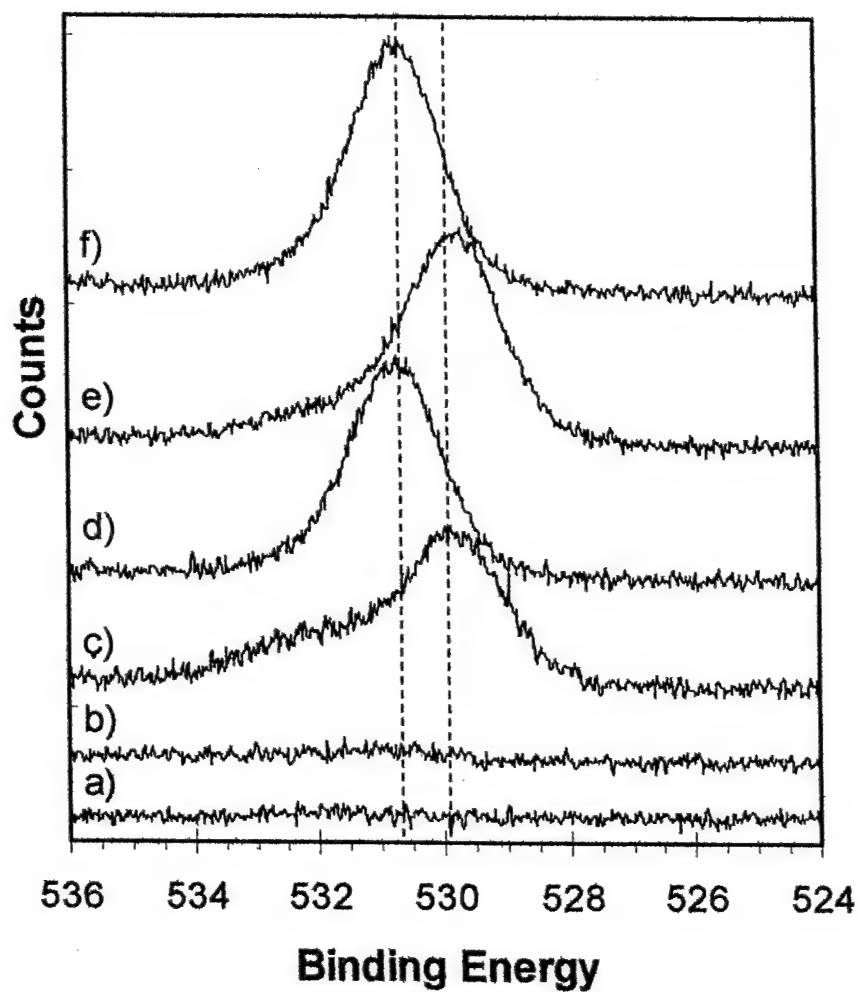


Figure 27. Oxygen 1s XPS spectra for: a) CVC Clean n-GaN, b) 4 Å Hf deposition, c) 4 Å Hf and O₂ plasma, d) 8 Å Hf, O₂ plasma, and 650°C anneal, e) 12 Å Hf and O₂ plasma, f) 650°C final anneal. The peak positions of the initial surface, as well as the final surface are indicated with dashed lines.

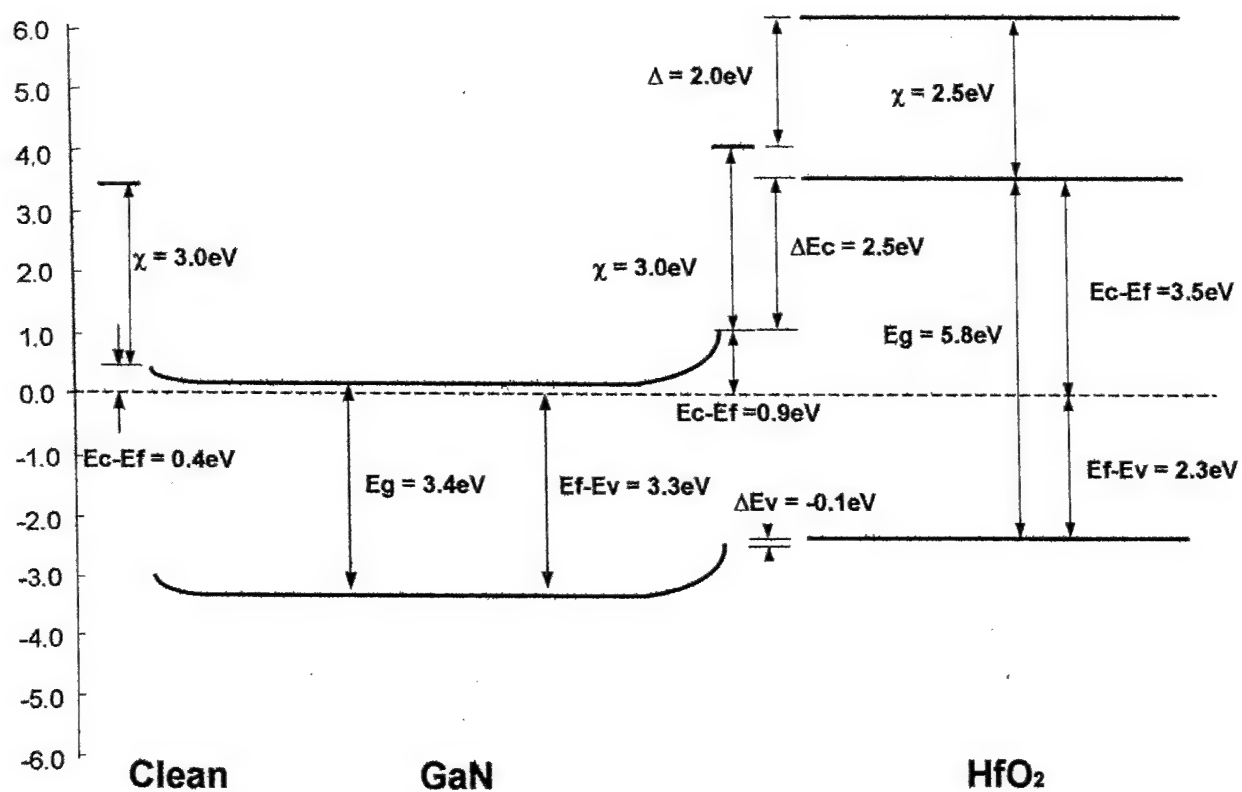


Figure 28. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and HfO₂ before annealing. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.

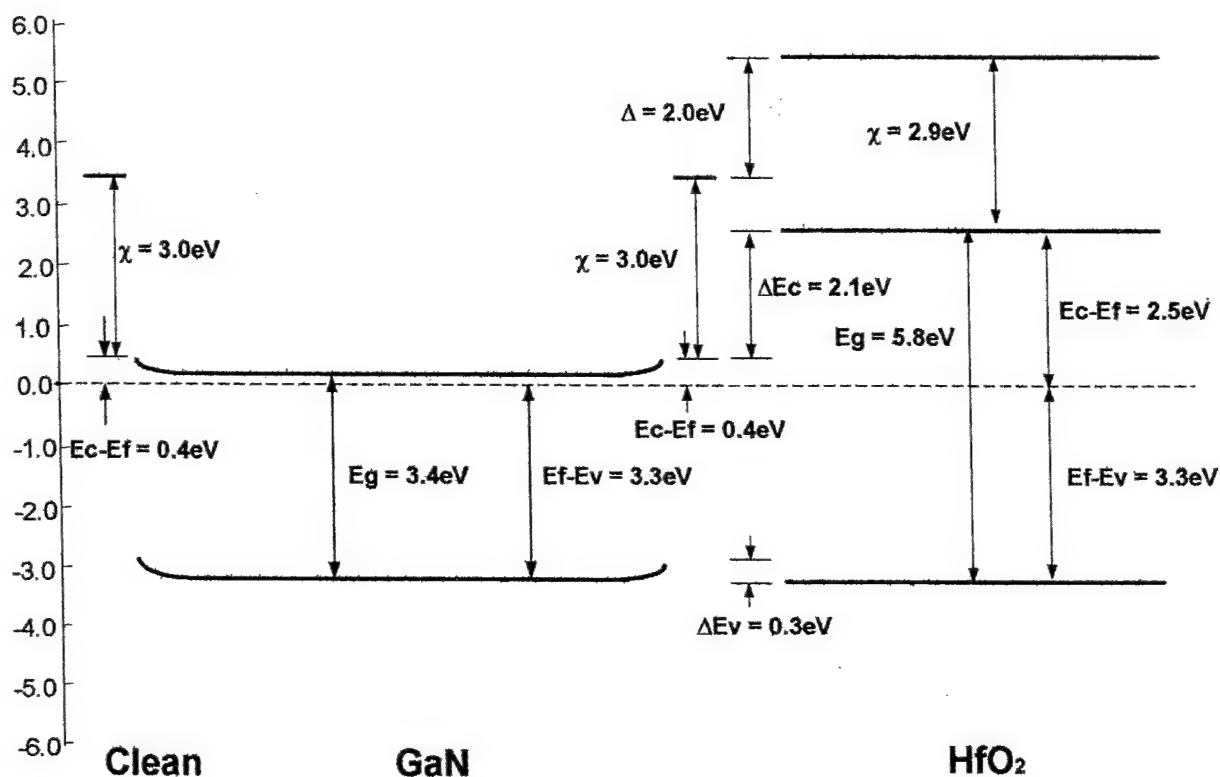


Figure 29. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and HfO₂ after annealing at 650 °C. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.

Significant Papers

There are several papers which summarize the significant research of this paper in detail. These are attached directly to this document in the pages that follow. In order of inclusion, these are:

- i) an MRS paper on GaN-SiO₂ band offset, included is the abstract;
- ii) a paper published in the JAP on GaN-SiO₂ band offsets;
- iii) a paper to be published in the JAP on GaN-Si₃N₄ band offsets;
- iv) a letter submitted to APL on GaN-HfO₂ band offsets;
- v) a paper to be published in Appl Surf Sci; and
- vi) two papers submitted to JVSTA on GaN plasma processed interfaces with SiO₂.

In addition, there are two PhD dissertations completely by Drs. Bae and Cook, respectively that can be accessed via the internet.

Dr. C Bae, PhD Dissertation, NC State University, May 2003.

Dr. T.E. Cook, PhD Dissertation, NC State University, May 2003.

The Cook thesis can be accessed by going the NC State Libraries search engine for theses and dissertations:

<http://www.lib.ncsu.edu/ETD-db/>

The Bae thesis will be on-line within the next 4-6 weeks.

Band Offset Measurements of Si_3N_4 on Clean n-type GaN

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The investigation of the band alignment of the Si_3N_4 -GaN interface is important for passivation of high voltage devices and possibly for gate insulator applications. In this study X-ray and UV photoelectron spectroscopy were used to measure the electronic states as Si_3N_4 was deposited on clean GaN surfaces. The n-type GaN ($5 \times 10^{18} \text{ cm}^{-3}$) surface was atomically cleaned in NH_3 at 860°C , and the surface showed upward band bending of $\sim 0.2 \pm 0.1 \text{ eV}$ with an electron affinity of $3.1 \pm 0.1 \text{ eV}$. Layers of Si ($\sim 0.2 \text{ nm}$) were deposited on the clean GaN which were nitrided using an ECR N_2 plasma at 300°C and subsequently annealed at 650°C for densification of the Si_3N_4 film. Surface analysis was performed after each step in the process, and yielded a valence band offset (VBO) of $\sim 0.6 \text{ eV}$, where the valence band of the GaN lies 0.6 eV below the Si_3N_4 valence band. This result may explain the rise in gate leakage current in HFETs. The conduction band offset (CBO) of $\sim 2.2 \text{ eV}$ is deduced from the measurement of the VBO and knowledge of the respective bandgaps. These values are in relative agreement with the predicted values of 0.7 eV and 2.3 eV for the VBO and CBO obtained from the charge neutrality level (CNL) model of the heterojunction interface.

Measurement of the band offsets of SiO₂ on clean n- and p-type GaN(0001)

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ABSTRACT

The band alignment at the SiO₂-GaN interface is important for passivation of high voltage devices and for gate insulator applications. X-ray photoelectron spectroscopy (XPS) and ultraviolet photoemission spectroscopy (UPS) have been used to observe the interface electronic states as SiO₂ was deposited on clean GaN (0001) surfaces. The substrates were metallorganic chemical vapor deposition (MOCVD) grown n-type (1×10^{17}) and p-type (2×10^{18}) GaN on 6H-SiC (0001) with an AlN (0001) buffer layer. The GaN surfaces were atomically cleaned via an 860°C anneal in an NH₃ atmosphere. For the clean surfaces, n-type GaN showed upward band bending of 0.3 ± 0.1 eV, while the p-type GaN showed downward band bending of 1.3 ± 0.1 eV. The electron affinity for n-type and p-type GaN was measured to be 2.9 ± 0.1 eV and 3.2 ± 0.1 eV, respectively. To avoid oxidizing the GaN, layers of Si were deposited on the clean GaN surface via UHV e-beam deposition, and the Si was oxidized at 300°C by a remote O₂ plasma. The substrates were annealed at 650°C for densification of the SiO₂ films. Surface analysis techniques were performed after each step in the process, and yielded a valence band offset (VBO) of 2.0 ± 0.2 eV and a conduction band offset (CBO) of 3.6 ± 0.2 eV for the GaN-SiO₂ interface for both p- and n-type samples. An interface dipole of 1.8 eV and 1.5 eV was deduced for the GaN-SiO₂ interface for the n-type and p-type surfaces, respectively.

I. Introduction

Gallium nitride is being investigated for a wide range of electronic and optoelectronic applications. In particular, the interfacial band alignment is of significant interest in the fabrication of devices based on heterostructures. The heterojunction band discontinuities are key parameters of device design because the valence and conduction band offsets determine the transport and confinement properties at the interface. A fundamental objective for technology and basic research would be the control of the band discontinuities¹. The deposition of SiO₂ on GaN could be important for passivation of high voltage devices and for the gate insulator in field effect transistor (FET) devices.² While the Si-SiO₂ interface has been studied extensively,³⁻⁷ little research has been reported and large uncertainties exist on the band offsets at nitride interfaces.⁸⁻¹²

Surface preparation is a critical step to controlled heterostructure formation. In prior studies Bermudez¹³ compared GaN surfaces prepared by sputtering with nitrogen ions followed by annealing in ultrahigh vacuum (UHV) and surfaces prepared by *in situ* deposition of Ga metal followed by thermal desorption. For the two processes, no significant differences of the values of work function, band bending and Ga 3d binding energy were found, which suggests that nitrogen-ion sputtering and annealing are equivalent for preparation of ordered GaN surfaces. However, surfaces prepared by these methods show additional emission at energies above the valence band maximum (VBM) in photoemission data that has been attributed to surface states. In our study, GaN is prepared by an *in situ* ammonia exposure at an elevated temperature,¹⁴ producing atomically clean surfaces without observable emission above the VB turn-on.

Several groups have reported the electrical characteristics of the plasma enhanced chemical vapor deposition (PECVD) grown SiO₂-GaN interface. Casey *et al*¹⁵ found no

observable hysteresis in room temperature C-V measurements, as well as an increase of capacitance with incident ultraviolet light while in deep depletion. These observations are consistent with a low concentration of interface traps. M. Sawada *et al*¹⁶ and Arulkumaran *et al*¹⁷ support this observation, measuring $1-2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ and $2.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, respectively for the minimum interface state density at the SiO₂-GaN interface. T. Sawada *et al*¹⁸ investigated the effect of thermal annealing of the interface. The interface state density was reduced 33% to $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ after annealing in H₂ at 500°C. Also noted was that the Fermi level was not pinned and could move within the upper band gap. The as-deposited sample had a Fermi level 0.2eV from the conduction band edge under thermal equilibrium conditions, and the value increased to 0.5eV after annealing. The relatively low interface trap density suggests the promise of applications for this interface. While several studies¹⁹⁻²¹ have employed photoemission techniques to explore metal/GaN interfaces, there has been, to our knowledge, no similar report for the SiO₂-GaN interface.

A first approach to describing a heterostructure interface is to apply the electron affinity model (EAM). This model holds in the ideal case, assuming there is no potential created as the heterostructure is formed. The alternative model is the interface dipole model, where the structure of the interface causes a shift in the entire band lineup relative to the predictions of the EAM. The well-known occurrence of reconstruction, chemical reaction, dislocation and strain at the interface may result in contributions to the so-called "structural interface dipole".²² The focus of our experiment is to measure the band offsets and to compare the results to this dipole at the heterostructure interface.

The charge neutrality level (CNL) model has been used to describe the band alignment of a heterojunction interface between two semiconductors. Tersoff²³ suggested that the band

alignment between two semiconductors is controlled by the charge transfer across the interface and the resulting interface dipoles in a fashion similar to Schottky barrier models. Recently, Robertson²⁴ employed the S parameter, which reflects the dielectric screening to relate the relative contribution of the electron affinity model and the dipole from the charge neutrality levels. In this study, correlation between the CNL model and experimental data will be presented.

In this study, *in situ* XPS and UPS measurements are used to determine the band discontinuities, or band offsets, at the GaN-SiO₂ interface. This process is a well-established method that has been reported in the literature.^{22,25,26} After achieving an atomically clean GaN (0001) surface, care is taken to avoid oxidation during the process. Our basic approach in this study is to obtain a clean GaN surface through an ammonia exposure at an elevated temperature and to form an SiO₂ layer by depositing silicon and to employ low temperature oxidation to minimize disruption of the interface. XPS and UPS measurements are obtained after each step of the process, and the band bending is deduced from the shifts of the gallium and nitrogen core levels. The band offsets and electron affinities are determined from the UPS spectra, and the formation of the oxide and the value of the interfacial dipole are determined from the XPS and UPS measurements.

II. Experimental Procedures

The GaN films used in this study were grown via metallorganic chemical vapor deposition (MOCVD) on 50 mm diameter on-axis Si-face, 6H SiC (0001) substrates with a conducting AlN (0001) buffer layer. The thickness of the GaN epilayer and the AlN buffer were 1.1 μm and 0.1 μm , respectively. Prior research has established that MOCVD growth of GaN on

Si face SiC(0001) results in Ga face GaN(0001).^{27,28} Silicon was used as the n-dopant, and magnesium was used as the p-dopant. Ionized donor concentrations ($N_d - N_a$) of $1 \times 10^{17} \text{ cm}^{-3}$ and $2 \times 10^{18} \text{ cm}^{-3}$ were measured for the n-type and p-type samples using capacitance-voltage measurements with a mercury probe.

Raman spectroscopy was employed to characterize the residual strain in the GaN film. The E_2 mode, which is employed to characterize the biaxial strain,²⁹ was found at 564.4 cm^{-1} . The E_2 mode is found at 567.2 cm^{-1} for a free standing film, and this value is used as the reference. Therefore, we deduce a residual tensile strain of 1.4×10^{-3} and a residual tensile stress of 0.6 GPa .³⁰

Ex situ preparation of the GaN consisted of a process where the films were cleaned sequentially in trichloroethylene, acetone, and methanol baths for 1 minute each, followed by immersion into 49% HCl for 10 minutes. The samples were then rinsed for 10 seconds in deionized water, and blown dry using nitrogen. The samples were mounted to molybdenum plates, secured by tantalum wires, and then placed in the load lock for entry into the transfer line that interconnects several analysis and processing chambers. The total time between the completion of *ex situ* cleaning and inserting into the system was about 10 minutes.

Initial surface analysis was performed, and the sample was moved to the gas source molecular beam epitaxy (GSMBE) for *in situ* cleaning. The cleaning process consists of annealing at 860°C for 15 minutes in an NH_3 atmosphere. Ammonia was introduced into the chamber when the temperature reached 500°C via a needle valve and a chamber pressure of 1×10^{-4} torr was obtained. The distance between the ammonia doser and sample was $\sim 5 \text{ cm}$, and the partial pressure of ammonia at the sample surface is expected to be as much as an order of magnitude higher than the system pressure. After allowing 5 minutes for the pressure to

stabilize, the heater was ramped to 860°C at a rate of 30°C per minute. The temperature and ammonia flow was maintained for 15 minutes. Subsequently, a ramp rate of -40°C per minute was used to achieve a heater temperature of 500°C; the sample was held at this temperature while the needle valve was closed. The pressure decreased to the low 10^{-8} torr range, during which the sample cooled to ~200°C, and was transferred out of the system.

After cleaning and other process steps, the samples were transferred in UHV for surface analysis. For XPS, a dual anode X-ray source was used to generate magnesium (1253.6eV) or aluminum (1486.6eV) X-rays, and the photoemitted electrons were analyzed with a Fisons Clam II operated at a resolution of 0.1eV. UPS with He I (21.2eV) radiation was employed to measure the electronic states near the valence band and to determine the electron affinity. The photoemitted electrons were analyzed with a VSW 50 mm mean radius hemispherical analyzer operated with a resolution of 0.1eV. A negative 4 V bias was applied to the sample to overcome the work function of the analyzer.

The XPS and UPS spectra were obtained after each process step in a sequence of experiments to follow the shifts of the XPS peaks and the evolution of the valence band spectra. The spectra were measured to track the peak shifts and discern the band bending and band offsets after each of the following steps: 2Å Si deposition, a second 2Å Si deposition (4Å total), O₂ plasma at 300°C, 2Å Si (6Å total Si) and O₂ plasma at 300°C, 650°C anneal for 15 minutes, a final 3Å Si deposition (9Å Si total) and O₂ plasma at 300°C, and a 15 minute 650°C final anneal. Throughout the manuscript, references to the Si thickness in the processing steps refer to the total amount of Si deposited up to that particular step. The ultimate thickness of the oxide film was calculated to be ~18Å using a density comparison method. This thickness was measured

experimentally to be $\sim 17\text{\AA}$ by examining the XPS core level intensities for the clean and final process steps.

III. Results

The evolution of the UPS spectra from the clean GaN through oxidation and anneal of the deposited 9\AA Si for the n-type experiment is shown in Figures 1 and 2. The VBM of the clean GaN surface was determined from an extrapolation of a line fit to the leading edge of the spectrum. A turn-on of the GaN signal was measured at $3.0 \pm 0.1\text{eV}$ (referenced to the Fermi level). From the doping concentration of 1×10^{17} in the GaN, the bulk Fermi level was determined to be $\sim 100\text{meV}$ below the conduction band minimum. Because the deposited layers obscure the valence band maximum, in order to follow the position of the VBM, it is necessary to detect a more intense bulk GaN spectral feature to reference the position of the VBM. A feature at 13.4eV in the spectra shown in Figure 1 has been attributed to a GaN bulk excitation.³¹ Note that this feature shifts to a higher binding energy by $0.3 \pm 0.1\text{eV}$ with the deposition of 4\AA of Si and the oxidation that followed. This shift is an indication of a reduction of the band bending by 0.3eV and is consistent with essentially flat band conditions after the oxidation. Tracking the peak movement is only possible when the substrate emission is observable, therefore when the layer thickness obscures this emission, no further information can be obtained. In our UPS measurements, emission from the substrate was not detected for the 9\AA silicon deposition and oxidation. With increased thickness, the turn-on and signature peaks for SiO_2 remained unchanged.

The spectra shown in Figure 1 were used to determine the electron affinity of GaN, as well as the deposited SiO_2 . The electron affinity can be determined by the relation:

$$\chi = h\nu - W - E_g \quad (1)$$

where W is the spectral width from the VBM to the low energy cut-off, $h\nu$ is the photon energy (21.2eV), and E_g is the bandgap of the material. For different cleaning procedures the VBM is sometimes obscured by surface states,^{13,32} but for this study we will employ the method noted above assuming it is representative of the VBM. For the clean GaN surface, the width of the spectrum was measured to be 14.9eV and 14.7eV for the n- and p-type, respectively. Using the generally accepted bandgap of GaN, 3.4eV, the electron affinity was determined to be 2.9eV and 3.1eV for the n- and p-type, respectively. While the electron affinity differs by 0.2eV between the two samples, this is within the experimental error and in agreement with prior reports of 3.0eV for GaN.^{13,20,33}

We employ the same approach to determine the electron affinity of the SiO₂ layer. The turn-on for the SiO₂ is observed at ~5.1eV below the Fermi level, and the spectral width is measured to be 11.1eV. Assuming a bandgap of 9.0eV, we obtain an electron affinity of 1.1eV, which is consistent with prior reports.²⁴

The scans shown in Figure 3 represent the evolution of the UPS spectra from the clean GaN through the final surface for the p-type substrate. Figure 4 presents an expanded scan of the clean surface, which indicates a VBM at 1.6eV (referenced to the Fermi level). Based on the $2 \times 10^{18} \text{ cm}^{-3}$ doping of the Mg, the bulk Fermi level is calculated to be ~300meV above the VBM. The GaN bulk feature observed at 12.2eV is in agreement with values reported elsewhere.¹⁹ This feature shifts to a higher binding energy by $0.9 \pm 0.1 \text{ eV}$ with the formation of the SiO₂ layer.

The evolution of the gallium 3d peak during the n-type GaN experiment is shown in Figure 5. The initial peak position and width of the peak for the clean surface was determined to

be $20.4 \pm 0.1 \text{ eV}$ and $1.35 \pm 0.1 \text{ eV}$, respectively. This peak position minus the VB turn-on is 17.4 eV , and is close to the value of 17.7 eV reported by Waldrop and Grant³⁴. In some data sets we have found values consistent with the 17.7 eV found by Waldrop and Grant.³⁴ In our case the core level and valence band measurements are made with two separate instruments and variations in calibration are likely responsible for the small differences. The primary considerations of our measurements are on relative peak shifts, so these small variations do not affect our analysis.

Spectra observed after the first and second 2 \AA Si depositions showed shifts that were smaller than 0.1 eV . After an anneal following the third 2 \AA Si deposition (6 \AA total) and oxidation, the peak shifted to $20.65 \pm 0.1 \text{ eV}$, while the width increased to $1.4 \pm 0.1 \text{ eV}$. For the final surface, which consisted of a 9 \AA Si layer that was oxidized, the peak was observed at $20.76 \pm 0.1 \text{ eV}$, indicating a shift of $0.36 \pm 0.1 \text{ eV}$ for the entire experiment. There are no indications of a reaction between the GaN and the SiO_2 , therefore suggesting that this shift is due to a change in the band bending.

Similar behavior was observed for the evolution of the nitrogen 1s core level. The N 1s peak position for the clean n-type GaN surface was observed at $397.9 \pm 0.1 \text{ eV}$, and the width was measured to be $1.1 \pm 0.1 \text{ eV}$. As in the case of the Ga 3d, the N 1s shifted a discernable amount after the third 2 \AA Si deposition (6 \AA total) and oxidation, to $398.2 \pm 0.1 \text{ eV}$, with a width of $1.2 \pm 0.1 \text{ eV}$. For the final surface, the peak shifted to $398.3 \pm 0.1 \text{ eV}$, with a width of $1.1 \pm 0.1 \text{ eV}$. This difference of $0.37 \pm 0.1 \text{ eV}$ is again consistent with values obtained for the gallium core level peaks.

Figure 6 displays the evolution of the oxygen 1s core level. As measured by XPS, the as-loaded GaN sample contains ~ 14 and 8 atomic percent of oxygen and carbon, respectively. The

chemical vapor clean (CVC) clean reduces the oxygen and carbon below the XPS detection limits (< 1 atomic percent).

The surface termination of the GaN after the CVC clean has not been determined. The Si 2p and N 1s core levels were examined for evidence of Si-N bonding immediately after the first silicon deposition. For the Si 2p, the nearby location of the Ga 3p core level, as well as the subtle difference in peak location for Si-O and Si-N bonding limited the ability to detect Si-N bonding. Similarly, we found that the N 1s core level in GaN and in Si_3N_4 deposited on GaN essentially overlap. With these considerations, we cannot exclude the possibility of Si-N at the surface even though no direct evidence was found in our measurements.

After deposition of 4\AA Si and the O_2 plasma, the initial peak position was observed at $532.2 \pm 0.1\text{eV}$. Through the course of the experiment, the peak shifted to 533.1eV , for a total of $0.9 \pm 0.1\text{eV}$. This peak only slightly deviates by 0.2eV from the 533.3eV value reported in the literature for SiO_2 on silicon substrates.^{36,37} The final peak position for the O 1s core level of the SiO_2 on p-type GaN is at 532.5eV , which is also generally consistent with the prior value.

The oxide quality is an important issue because it affects the bandgap of the material. Careful comparisons were made of the oxide grown on the GaN surface to SiO_2 grown on silicon. The difference in energy between the O 1s and Si 2p core levels was found to be 429.5eV in the oxide grown in our experiment, which is equivalent with the value found in the literature.³⁸ This finding suggests that the quality of our film is consistent with SiO_2 grown on Si.

Figure 7 shows the O 1s core level for p-type GaN CVC cleaned, oxidized and SiO_2 surfaces. The oxidized GaN surface has a peak position of 530.2eV . The SiO_2 surface shown is that of the final surface of the p-type experiment, and has a peak position of 532.5eV . The Ga-O

bond found in the oxidized case could not be resolved in the SiO_2 spectra. The Ga 3p core level has a higher surface sensitivity than the Ga 3d core level, and is shown in Tables I and II for the n- and p-type experiments. The Ga 3p core level displays shifts that are consistent with those of the Ga 3d and N 1s core levels, without indication of a chemical shift due to Ga_2O_3 formation. As mentioned previously, the SiO_2 formed on the surface is shown to have a limited reaction with the GaN and is below the detection limits in XPS.

Further evidence of SiO_2 formation can be detected in the silicon 2p peak spectra. After Si deposition, the initial peak position was observed at $101.59 \pm 0.1 \text{ eV}$. This peak shifted to $103.61 \pm 0.1 \text{ eV}$ after oxidation and subsequent annealing of the substrate. This peak position, as well as the shift of 2 eV, is consistent with SiO_2 on Si substrates,³⁹ which we attribute to a chemical shift due to the formation of SiO_2 .

The evolution of the gallium 3d peak for the p-type GaN experiment is shown in Figure 8. The initial peak position for the clean surface was observed at $19.18 \pm 0.1 \text{ eV}$. After the 4 Å Si deposition and oxidation, the peak shifted to a value of $19.4 \pm 0.1 \text{ eV}$. While the peak shifted $\sim 0.2 \text{ eV}$ during the oxidation, the largest shift occurred after each anneal of the sample, as evidenced by the peak positions of the 6 Å total Si/ O_2 plasma/650°C anneal and the 9 Å total Si/ O_2 plasma/650°C anneal treatments shown at $19.95 \pm 0.1 \text{ eV}$ and $20.05 \pm 0.1 \text{ eV}$, respectively. Annealing is a well-documented process for densification of the deposited oxide, which enhances the quality of the film.⁴⁰⁻⁴² During the course of the experiment we observed a shift in the spectra of $0.87 \pm 0.1 \text{ eV}$. The lack of a Ga-O peak in the spectra once again suggests a very limited reaction between the GaN and the SiO_2 , implying that this shift is due to a change in the band bending.

The peak position of the nitrogen 1s core level on the clean p-type GaN surface was observed at $396.65 \pm 0.1 \text{ eV}$, while the final position was $397.5 \pm 0.1 \text{ eV}$. This difference of $0.85 \pm 0.1 \text{ eV}$ is in excellent agreement with values for the Ga 3d levels.

The spectral peak positions and the full width-half maximum (FWHM) of the Ga 3p_{3/2}, Si 2p, O 1s, Ga 3d, and N 1s have been summarized in Tables I and II for both n and p-type GaN, respectively. From the results, two important properties of the interface can be stated. First, there does not appear to be a significant reaction at the GaN-SiO₂ interface. If this reaction were significant, there would be additional peaks reflecting the reacted environment, and/or changes in the widths of the peaks. Second, the observed shift for the Ga 3p_{3/2}, Ga 3d, and N 1s core levels are essentially the same, allowing the inference that the shifts are a result of band bending.

IV. Discussion

The method for determining the valence band discontinuity is similar to that of Waldrop and Grant³⁴ and Kraut *et al.*⁴³ Their basic approach is to reference the VBM to a core level in the XPS spectra for each semiconductor and to use the measured difference between the core level energies to discern the band discontinuities. In our study, we have employed UPS to measure the energy of the VBM from the Fermi level, and XPS is used to measure core level energies relative to the Fermi level.

Care was taken to avoid oxidation of the clean GaN surface after the CVC clean. A significant Ga₂O₃ layer at the interface can be a source of deep acceptors and interface states that can be detrimental to device fabrication.⁴⁴ Although gallium oxide was not observed within our detection limits, we expect that Ga-O bonding exists at the SiO₂-GaN interface. Therrien *et al.*⁴⁵

reported the significance of an ultra-thin Ga_2O_3 layer formation, which allowed a redistribution of electronic charge and reduction of the interfacial defect density.

The Ga face GaN (0001) is a polar surface, and the spontaneous polarization will lead to a negative bound charge at the GaN film surface and a positive bound charge at the back substrate interface. The GaN is also piezoelectric, but because the films are grown above the critical thickness there is only a small residual strain, and the piezoelectric induced polarization ($P_{pz}=0.002\text{C/m}^2$) is small in comparison to the spontaneous polarization ($P_{sp}=0.033\text{C/m}^2$).⁴⁶ The piezoelectric polarization for biaxial tensile strain contributes in the same direction as the spontaneous polarization. The negative surface bound charge is compensated by surface states and screened by ionized donors while the positive bound charge at the substrate interface is screened by the free carriers. The polarization bound charge screened by the ionized donors would lead to upward band bending at the GaN surface. We note that the XPS measurements of the Ga and N core levels would be shifted by the polarization fields, but all measurements of the band offsets are made relative to these values, and thus the measured band offsets should not be affected by polarization induced band bending. Moreover, since the strain is relatively small, the effect of strain on the band offsets is anticipated to be less than the experimental uncertainties in our measurements.⁴⁷

Figure 9 shows the proposed band lineups for the n-type GaN-SiO₂ interface. The decrease of 0.3eV band bending from the clean surface indicates essentially flat band conditions are achieved. The valence band offset determination is the measured UPS turn-on for SiO₂ (5.3eV), minus the GaN turn-on (3.0eV), minus the band bending (0.3eV). With this value and the knowledge of the bandgap of the material, the conduction band offset is obtained. The bandgap of SiO₂ has been widely reported to be 9.0eV⁴⁸⁻⁵⁰, and this value was used for the conduction band offset and electron affinity calculations. From our experiment, the valence band offset is deduced to be 2.0eV, and the conduction band offset is 3.6eV.

The p-type GaN-SiO₂ band lineup is represented in Figure 10. For the clean surface, the measured downward band bending and electron affinity were calculated to be 1.3 ± 0.1 eV and 3.2 ± 0.1 eV, respectively, assuming the Mg acceptor level lies ~ 300 meV above the VBM and a room temperature bandgap of 3.4 eV.⁵¹ Using the considerations mentioned above, the valence band offset was calculated to be 2.0 eV, and the conduction band offset of 3.6 eV.

The electron affinity levels for GaN and SiO₂ are represented in Figures 9 and 10. The electron affinity model of heterojunction formation predicts these levels to align at the interface. Our results show a deviation from the electron affinity model of 1.8 eV for the n-type GaN substrate and 1.5 eV for the p-type GaN substrate.

The electron affinity model is based on the premise that the interface is formed without disruption of the surface electronic states of either of the two materials. All reference is to the vacuum levels of the two materials. The measured difference between the prediction of the electron affinity model and the experimentally observed band offset represents a change in the interface dipole. In general, it is not possible to assign a specific interface dipole to the heterostructure, but it is reasonable to consider the change in interface dipole from that deduced by the electron affinity model. However, the relation to the vacuum level in the first place is somewhat arbitrary. While the electron affinity of a surface can be determined following the approach employed in this study, it is dependent on the details of the surface structure where surface reconstruction, steps, and adsorbates can cause changes of the electron affinity by several eV. Moreover, after interface formation, the vacuum level of the materials at the interface is not defined or measurable, and the interface structure may have little relation to the specific bonding of the free surface that was responsible for the value of the electron affinity.

As an alternative to the electron affinity model, it has been proposed that heterojunction band alignments are determined by alignment of the charge neutrality levels (CNL) of the two materials. The charge neutrality levels represent the branch point of the surface or interface states related to the valence or conduction band. Thus a neutral interface would have a Fermi level at the branch point. The presumption is that charge can transfer between the interface states of the two materials, which will cause an interface dipole. If the density of states is high or if the CNL of the two semiconductors are at similar relative energies, then the band offset will be determined by the relative position of the CNL of the two materials.

Recently, Robertson²⁴ adapted the interface defect model presented by Cowley and Sze⁵² to employ the CNL as the pinning levels. The model was applied to analyze the band alignment of a range of oxides on silicon, and the model seems consistent with most experimental results. In this model, charge transfer across the interface creates a dipole, which modifies the band lineup given by the electron affinity rule and is described by the relation:

$$\varphi_{CBO} = (\varphi_{CNL,a} - \varphi_{CNL,b}) - (E_{g,a} - E_{g,b}) + S\{(\chi_a - \chi_b) + (E_{g,a} - E_{g,b}) - (\varphi_{CNL,a} - \varphi_{CNL,b})\} \quad (2)$$

Where φ_{CBO} is the CBO, χ and φ_{CNL} are the electron affinities and charge neutrality levels for each semiconductor (a and b), and S is a pinning factor based on the dielectric properties of the materials. Here, the φ_{CNL} are defined relative to the VBM of each semiconductor. A value of $S=1$ represents the EAM while a value of 0 represents pinning at the CNL levels. To our knowledge, the CNL of SiO_2 has not been reported, and because of the high value of S for the SiO_2 -Si interface (0.86),²⁴ we cannot use the experimental results of the Si/SiO₂ interface to reliably place the SiO₂ CNL.

In an attempt to understand the relation of our measured band alignment and the different models for heterostructure band alignment, we have compared our measured interface

alignments to experimental results for SiO_2 on Si and SiO_2 on SiC in Figure 11. In each case the diagrams are aligned to the vacuum level at the SiO_2 , which has been measured to be at the same energy relative to the oxide bands. The bandgap of each material is indicated, as is the VBO. The position of the vacuum level of the clean surface of the semiconductor is indicated, and the difference between these values and the surface vacuum level is the deviation from the EAM. This difference represents the change in the interface dipole, and was found to be 0.5, 1.1, and 1.6 eV for SiO_2 on Si, SiC and GaN, respectively.

Also indicated in Figure 11 is the CNL of the semiconductors based on prior reports.^{24,53} We find that the CNL of the Si and the GaN are in relative alignment with respect to the SiO_2 band gap, but the CNL of the SiC falls substantially below these values. The variation of the CNL model for these three interfaces may be anticipated by the wide bandgap and the high value of S of the SiO_2 .

The progression of the interface dipole deduced from the deviation from the EAM is most likely related to the changes at the semiconductor surface since the oxide is the same in all cases. For the SiO_2/Si interface, the surface reconstruction of the Si is not expected to survive the bonding and this effect alone could account for the change in the interface dipole. The same might be true for the SiO_2/SiC interface where the increased interface dipole could also represent the charge transfer from the Si to the nearest neighbor C atoms. For both Si and SiC, the oxide interface layer is expected to contain Si-O bonding. For the SiO_2/GaN interface, Ga-O bonding is expected at the interface. With the Ga atomic layer more positive and the O layer more negative, the interface dipole would be expected to lower the GaN electronic levels with respect to the SiO_2 levels, which is consistent with our observations.

V. Conclusions

The band alignment of an SiO_2 layer on $1 \times 10^{17} \text{ cm}^{-3}$ n-type and $2 \times 10^{18} \text{ cm}^{-3}$ p-type GaN has been investigated. Annealing in ammonia at 860°C provided atomically clean, stoichiometric GaN surfaces with $0.3 \pm 0.1 \text{ eV}$ upward band bending and $1.3 \pm 0.1 \text{ eV}$ downward band bending for the n-type and p-type surfaces, respectively. The electron affinity for the clean n-type and p-type GaN surfaces was measured to be 2.9 eV and 3.2 eV , respectively. After careful formation of the GaN- SiO_2 interface, flat bands were observed in the n-type experiment, while an additional 0.9 eV downward band bending was observed for the p-type experiment. For both measurements, a valence band offset of $2.0 \pm 0.1 \text{ eV}$ was obtained, while the conduction band offset was determined to be $3.6 \pm 0.1 \text{ eV}$ (assuming $E_{\text{g SiO}_2} = 9.0 \text{ eV}$). The interface dipole deduced from comparison with the electron affinity model was 1.8 eV and 1.5 eV for the n-type and p-type surfaces, respectively.

Acknowledgements

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Table I. XPS core level curve fitting results for the n-type GaN experiment.

Process Step	Ga 3p _{3/2}		Si 2p		O 1s		Ga 3d		N 1s	
	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)
CVC	105.71	2.69	-	-	-	-	20.41	1.35	397.90	1.10
2Å Si	105.71	2.67	101.59	3.72	-	-	20.48	1.35	398.02	1.12
4Å Si	105.71	2.68	100.90	2.87	-	-	20.46	1.35	398.01	1.13
O-PI	105.73	2.66	102.71	2.26	532.19	1.94	20.45	1.40	398.01	1.29
6Å Si, O-PI	105.89	2.68	102.95	2.06	532.37	1.85	20.56	1.44	398.05	1.26
Anneal	106.01	2.65	103.54	2.15	532.81	1.76	20.65	1.41	398.16	1.14
9Å Si, O-PI	106.03	2.68	103.59	1.92	533.10	1.77	20.74	1.37	398.25	1.11
Final	106.10	2.54	103.61	1.98	533.10	1.77	20.76	1.37	398.27	1.14
Difference	0.39		2.02		0.91		0.35		0.37	

Table II. XPS core level curve fitting results for the p-type GaN experiment.

Process Step	Ga 3p _{3/2}		Si 2p		O 1s		Ga 3d		N 1s	
	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)
CVC	104.53	2.81	-	-	-	-	19.18	1.64	396.65	1.34
4Å Si	104.8	2.91	99.8	3.81	531.34	2.57	19.55	1.66	396.93	1.31
O-PI	104.74	2.51	102.42	2.45	531.83	2.02	19.4	1.61	396.8	1.33
6Å Si, O-PI	104.86	2.70	102.84	2.46	531.94	1.92	19.42	1.63	396.82	1.36
Anneal	105.37	2.77	103.3	1.74	532.36	1.58	19.95	1.66	397.35	1.37
9Å Si, O-PI	104.72	2.98	102.68	1.90	532.0	1.80	19.48	1.61	396.9	1.27
Final	105.41	2.85	103.34	1.95	532.53	1.52	20.05	1.72	397.5	1.36
Difference	0.88		3.54		1.19		0.87		0.85	

FIGURE CAPTIONS

1. UPS spectra of a) CVC clean n-type GaN, b) 2Å Si, c) 4Å Si and O₂ plasma, d) 6Å Si, O₂ plasma and 650°C anneal, e) 9Å Si and O₂ plasma, f) 650°C anneal.
2. UPS spectra of the valence band maximum of: a) CVC clean n-type GaN, b) 2Å Si, c) 4Å Si and O₂ plasma, d) 6Å Si, O₂ plasma and 650°C anneal, e) 9Å Si and O₂ plasma, f) 650°C anneal.
3. UPS spectra of the valence band maximum of: a) CVC clean p-type GaN, b) 4Å Si and O₂ plasma, c) 6Å Si and O₂ plasma, d) 6Å Si, O₂ plasma and 650°C anneal, e) 9Å Si and O₂ plasma, f) 650°C final anneal.
4. UPS spectra of the valence band maximum of CVC clean p-type GaN, with valence band maximum indicated by a dashed line.
5. Gallium 3d XPS spectra for: a) CVC Clean n-type GaN, b) 2Å Si deposition, c) 4Å Si deposition, d) 4Å Si and O₂ plasma, e) 6Å Si, O₂ plasma, f) 6Å Si, O₂ plasma and 650°C anneal, g) 9Å Si and O₂ plasma, h) 650°C final anneal. The peak positions of the initial surface, as well as the final surface are indicated with dashed lines.
6. Oxygen 1s XPS spectra for: a) CVC Clean n-type GaN, b) 2Å Si deposition, c) 4Å Si deposition, d) 4Å Si and O₂ plasma, e) 6Å Si, O₂ plasma, f) 6Å Si, O₂ plasma and 650°C anneal, g) 9Å Si and O₂ plasma, h) 650°C final anneal. The peak positions after the initial oxidation, as well as the final surface are indicated with dashed lines.
7. Oxygen 1s XPS spectra for: a) CVC Clean p-GaN, b) O₂ Plasma, and c) the final SiO₂ surface. Dashed lines indicate the peak positions for the oxidized GaN, as well as the final SiO₂ surface.

8. Gallium 3d XPS spectra for: a) CVC Clean p-type GaN, b) 4Å Si deposition, c) 4Å Si and O₂ plasma, d) 6Å Si, O₂ plasma, e) 6Å Si, O₂ plasma and 650°C anneal, f) 9Å Si and O₂ plasma, g) 650°C final anneal. The peak positions of the initial surface, as well as the final surface are indicated with dashed lines.

9. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and SiO₂. The valence band offset, conduction band offset, band bending, and interface dipole are represented.

10. Deduced bands for the clean p-type GaN surface (left) and the interface between p-type GaN and SiO₂. The valence band offset, conduction band offset, band bending, and interface dipole are represented.

11. Band alignment of Si/SiO₂, SiC/SiO₂, and GaN/SiO₂ interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the SiO₂ surface, which is common in all three interfaces. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap. The VBO are determined from the measurements.

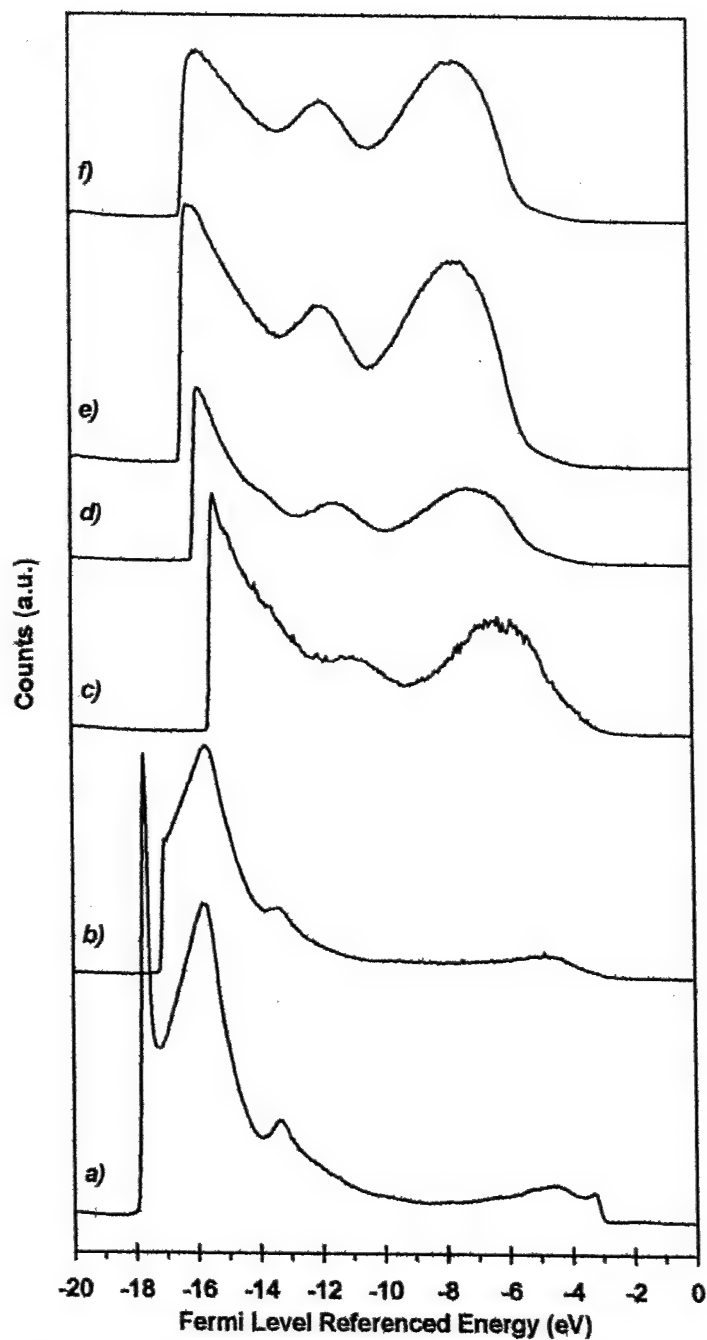


Figure 1. UPS spectra of a) CVC clean n-GaN, b) 2 Å Si, c) 4 Å Si and O₂ plasma, d) 6 Å Si, O₂ plasma and 650°C anneal, e) 9 Å Si and O₂ plasma, f) 650°C anneal.

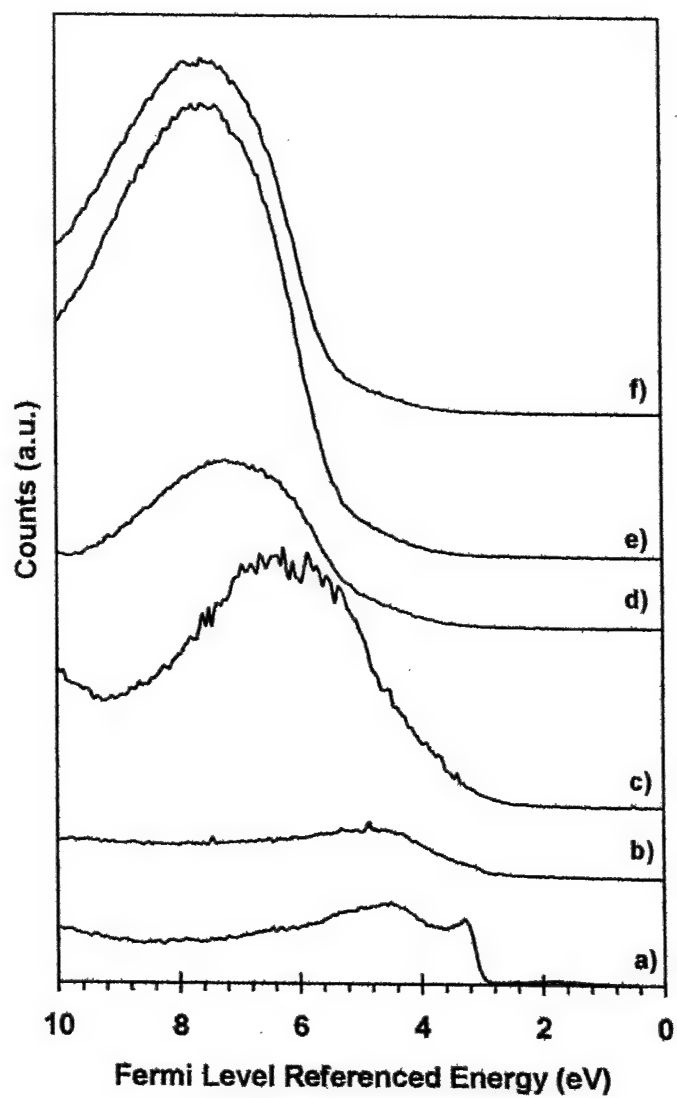


Figure 2. UPS spectra of the valence band maximum of: a) CVC clean n-GaN, b) 2 Å Si, c) 4 Å Si and O₂ plasma, d) 6 Å Si, O₂ plasma and 650°C anneal, e) 9 Å Si and O₂ plasma, f) 650°C anneal.

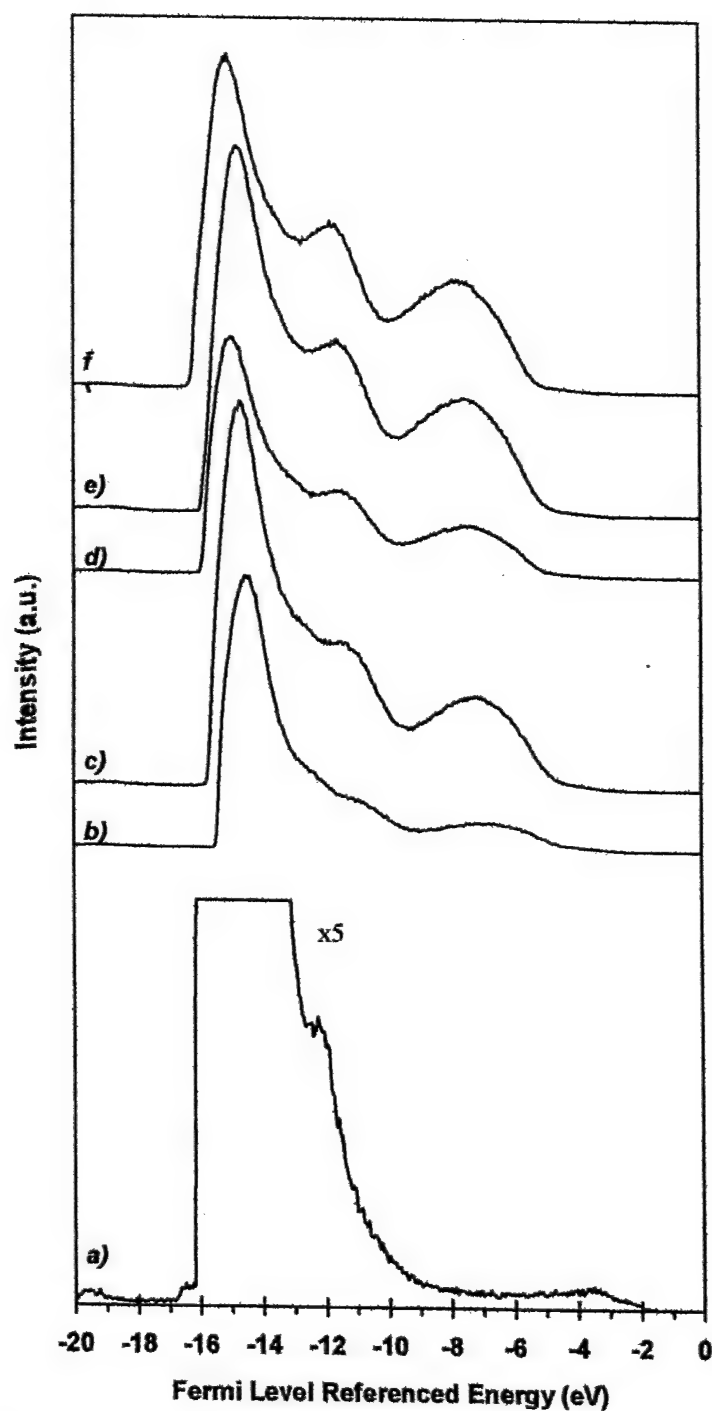


Figure 3. UPS spectra of the valence band maximum of: a) CVC clean p-GaN, b) 4 Å Si and O₂ plasma, c) 6 Å Si and O₂ plasma, d) 6 Å Si, O₂ plasma and 650°C anneal, e) 9 Å Si and O₂ plasma, f) 650°C final anneal.

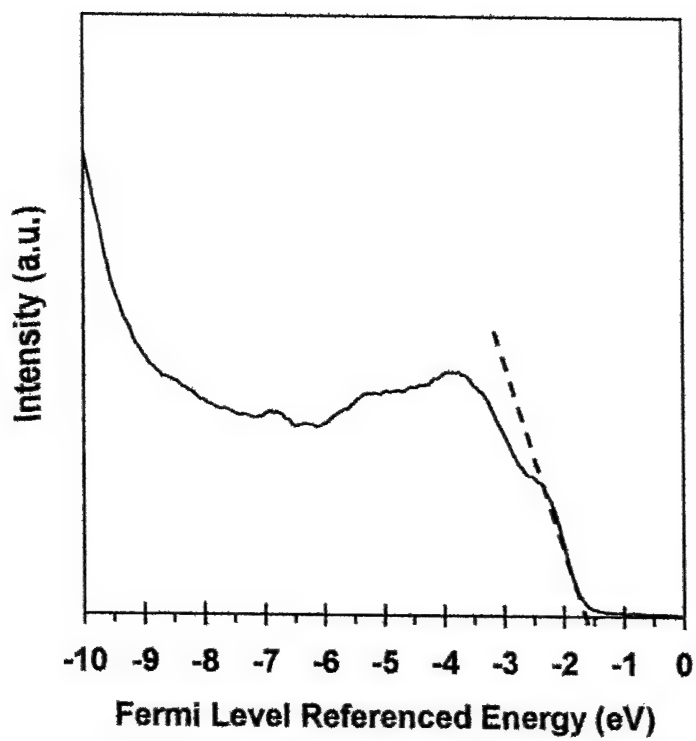


Figure 4. UPS spectra of the valence band maximum of CVC clean p-GaN, with valence band maximum indicated by a dashed line.

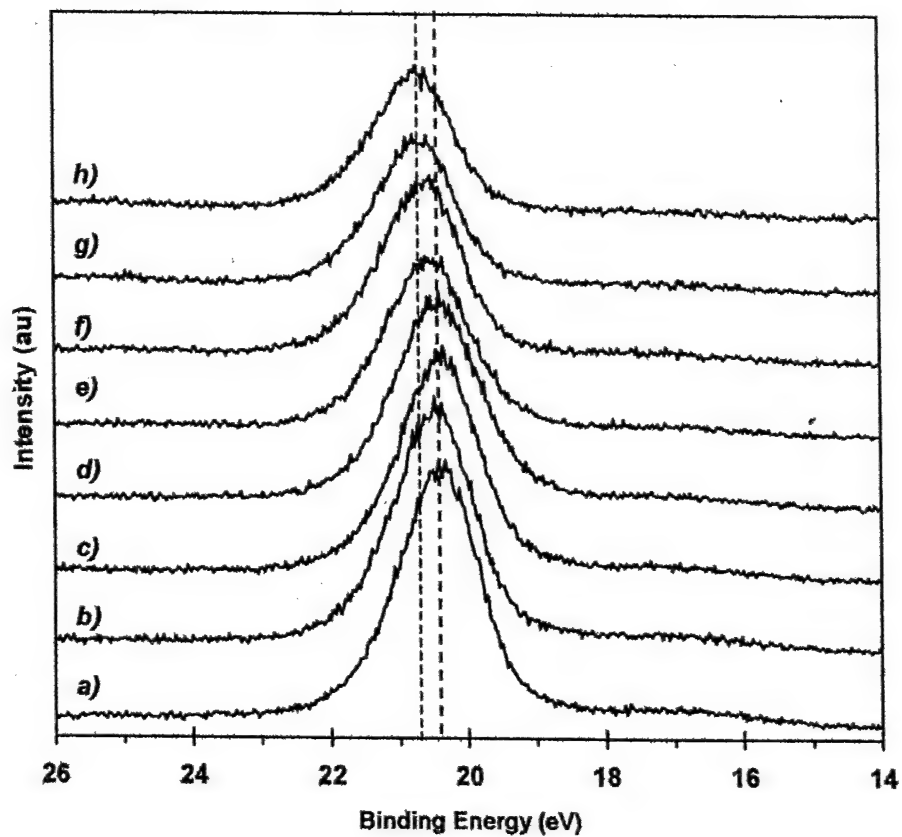


Figure 5. Gallium 3d XPS spectra for: a) CVC Clean n-GaN, b) 2Å Si deposition, c) 4Å Si deposition, d) 4Å Si and O₂ plasma, e) 6Å Si, O₂ plasma, f) 6Å Si, O₂ plasma and 650°C anneal, g) 9Å Si and O₂ plasma, h) 650°C final anneal. The peak positions of the initial surface, as well as the final surface are indicated with dashed lines.

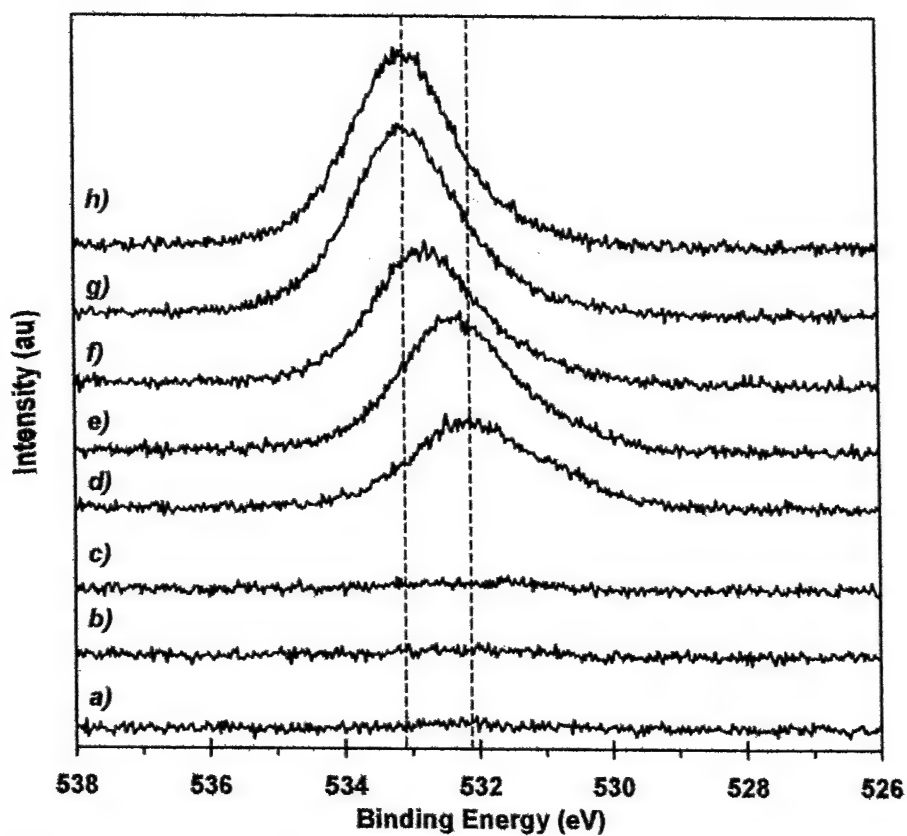


Figure 6. Oxygen 1s XPS spectra for: a) CVC Clean n-GaN, b) 2 Å Si deposition, c) 4 Å Si deposition, d) 4 Å Si and O₂ plasma, e) 6 Å Si, O₂ plasma, f) 6 Å Si, O₂ plasma and 650°C anneal, g) 9 Å Si and O₂ plasma, h) 650°C final anneal. The peak positions after the initial oxidation, as well as the final surface are indicated with dashed lines.

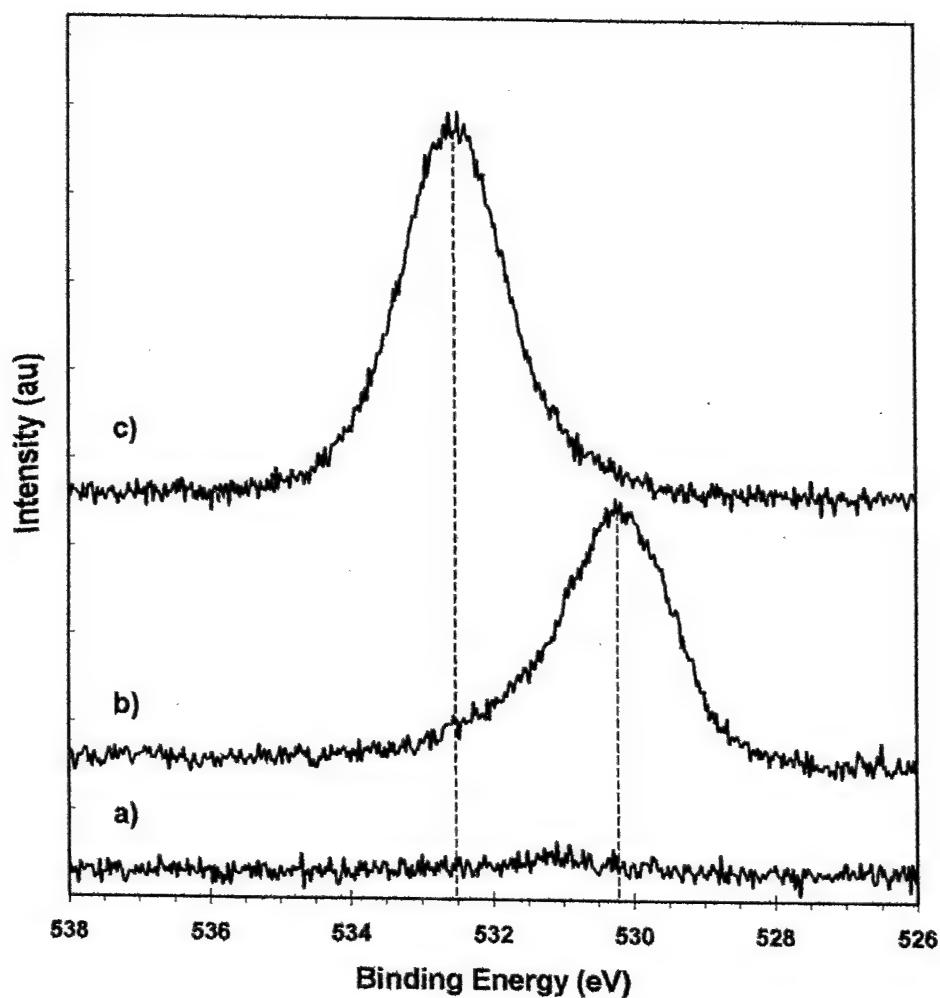


Figure 7. Oxygen 1s XPS spectra for: a) CVC Clean p-GaN, b) O₂ plasma, and c) the final SiO₂ surface. Dashed lines indicate the peak positions for the oxidized GaN, as well as the final SiO₂ surface.

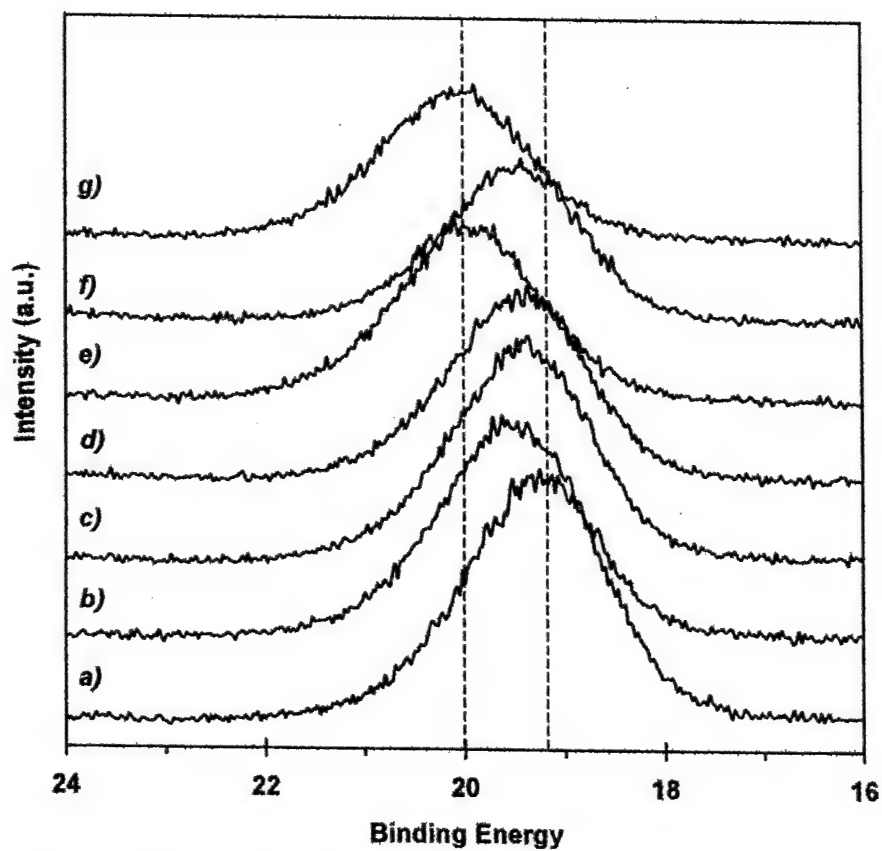


Figure 8. Gallium 3d XPS spectra for: a) CVC Clean p-GaN, b) 4 Å Si deposition, c) 4 Å Si and O₂ plasma, d) 6 Å Si, O₂ plasma, e) 6 Å Si, O₂ plasma and 650°C anneal, f) 9 Å Si and O₂ plasma, g) 650°C final anneal. The peak positions of the initial surface, as well as the final surface are indicated with dashed lines.

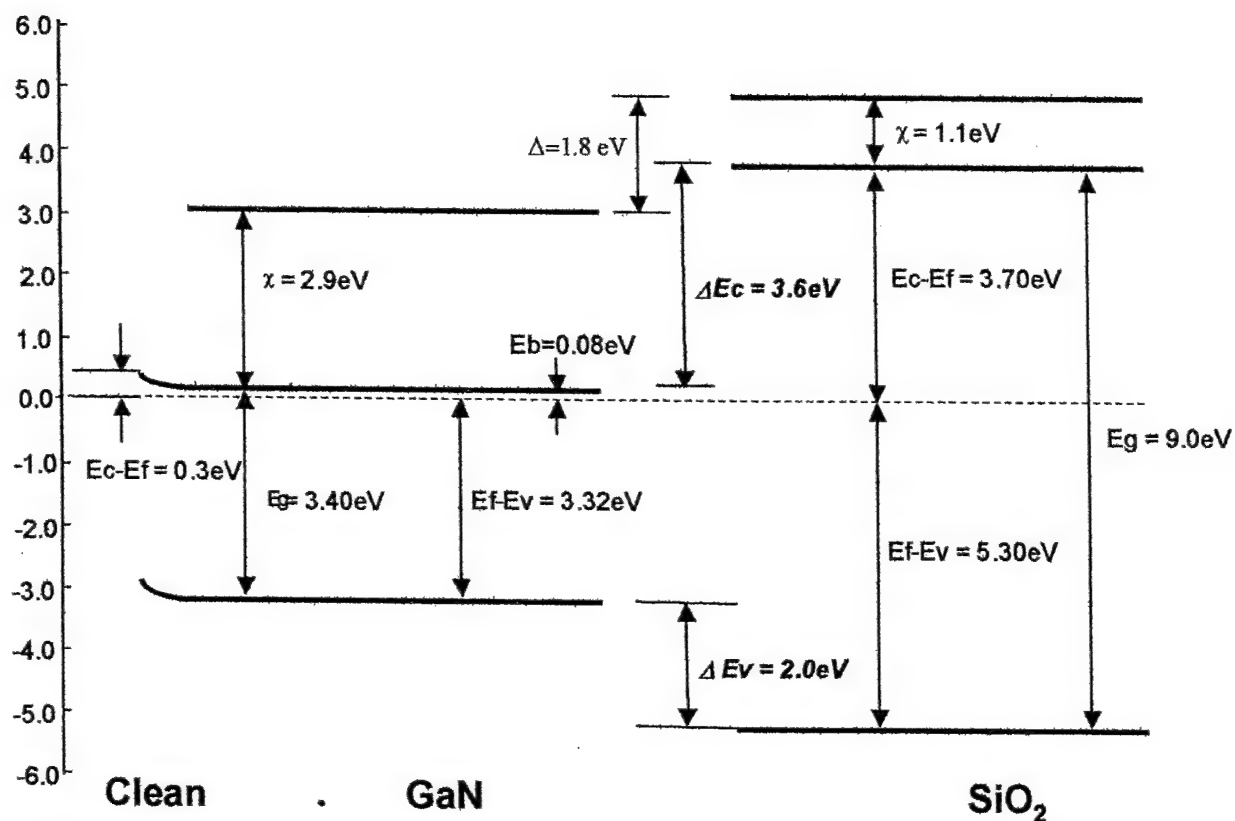


Figure 9. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and SiO₂. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.

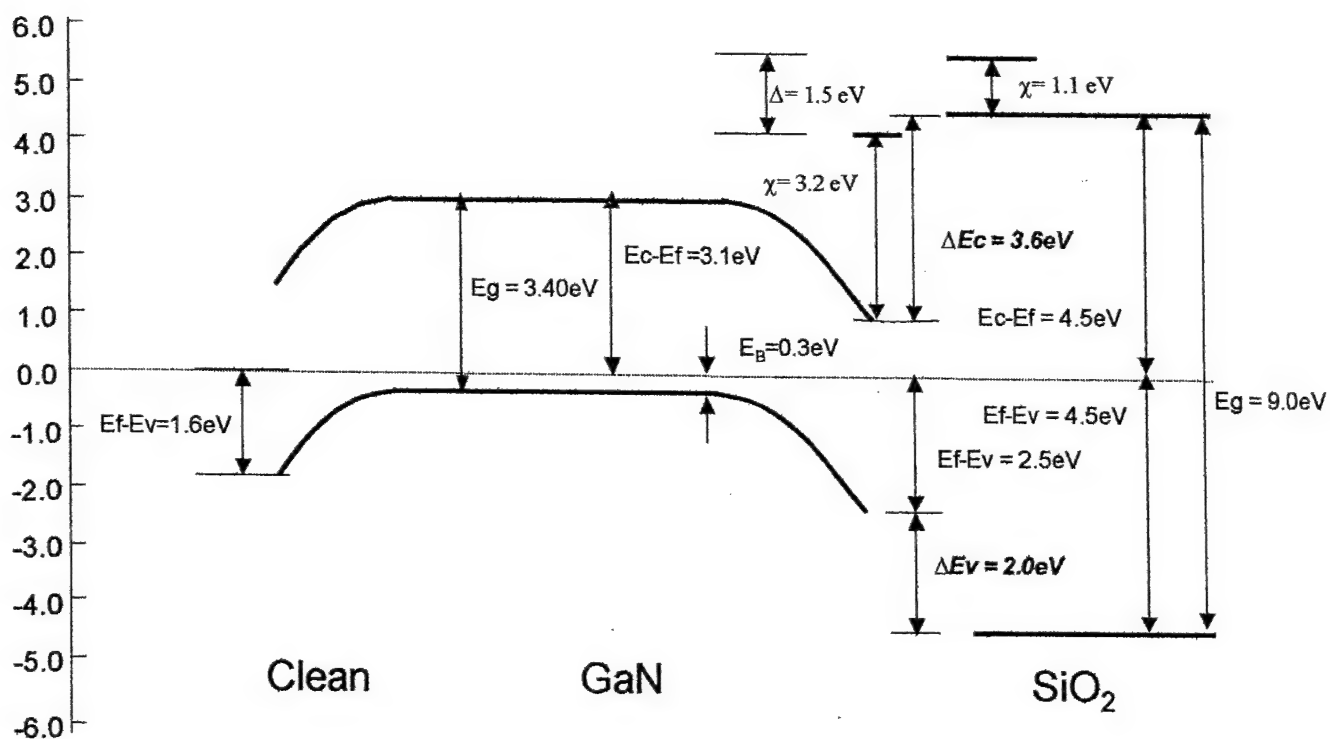


Figure 10. Deduced bands for the clean p-type GaN surface (left) and the interface between p-type GaN and SiO₂. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.

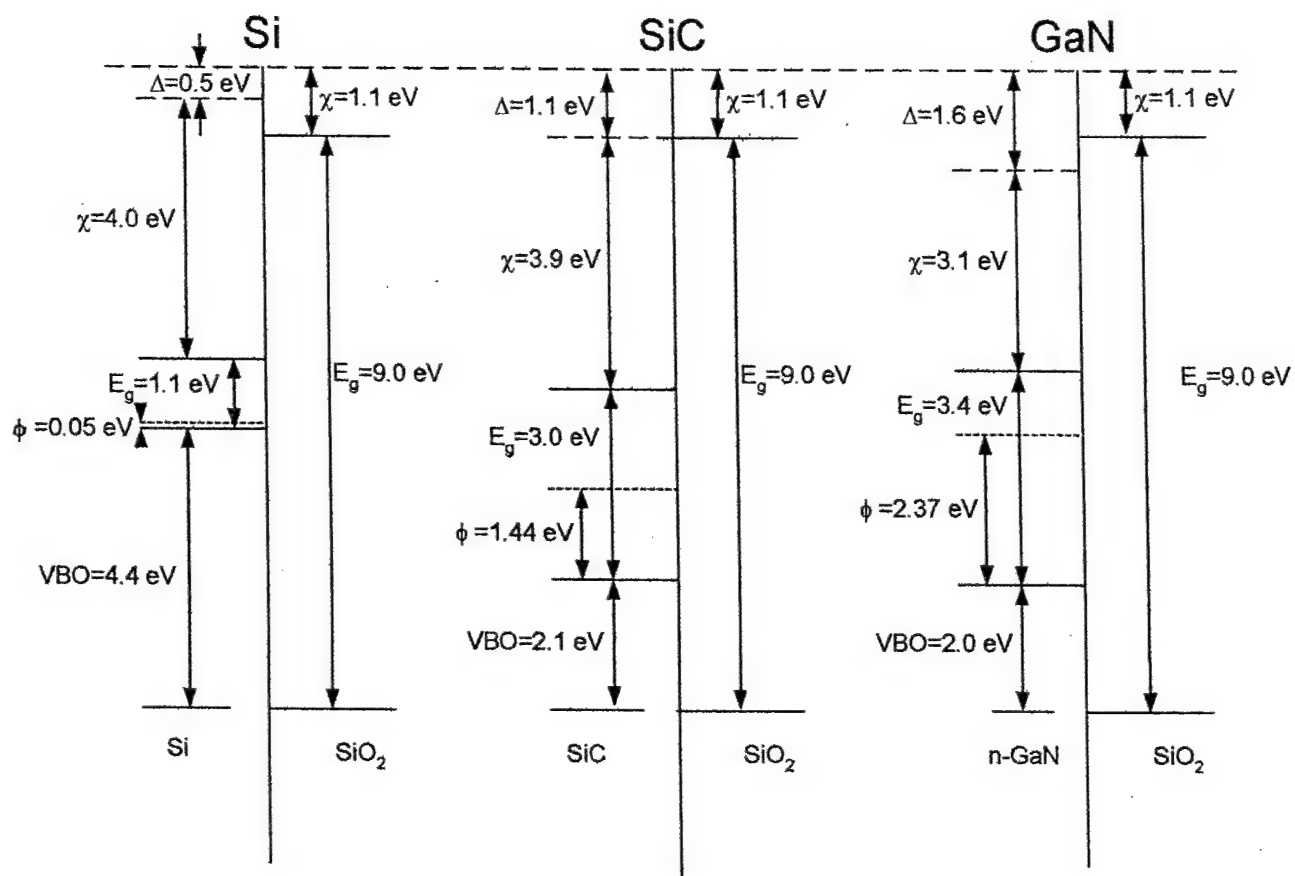


Figure 11. Band alignment of Si/SiO₂, SiC/SiO₂, and GaN/SiO₂ interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the SiO₂ surface, which is common in all three interfaces. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap. The VBO are determined from the measurements.

Band offset measurements of the $\text{Si}_3\text{N}_4/\text{GaN}$ (0001) interface

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ABSTRACT

X-ray photoelectron spectroscopy (XPS) and UV photoelectron spectroscopy (UPS) were used to measure the electronic states as Si_3N_4 was deposited on clean GaN (0001) surfaces. The n-type (2×10^{18}) and p-type (1×10^{17}) GaN surfaces were atomically cleaned in NH_3 at 860°C , and the n- and p-type surfaces showed upward band bending of $\sim 0.2 \pm 0.1$ eV and downward band bending of 1.1 ± 0.1 eV, respectively, both with an electron affinity of 3.1 ± 0.1 eV. Layers of Si (~ 0.2 nm) were deposited on the clean GaN and nitrided using an electron cyclotron resonance (ECR) N_2 plasma at 300°C and subsequently annealed at 650°C for densification into a Si_3N_4 film. Surface analysis was performed after each step in the process, and yielded a valence band offset (VBO) of $0.5\text{eV} \pm 0.1$ eV. Both interfaces exhibited type II band alignment where the valence band maximum of the GaN lies below that of Si_3N_4 valence band. The deduced conduction band offset (CBO) is found to be 2.4 ± 0.1 eV, and a change of the interface dipole of 1.1 ± 0.1 eV was observed for the $\text{Si}_3\text{N}_4/\text{GaN}$ interface formation.

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I. Introduction

Gallium nitride has been established as a material of choice for high frequency electronic and optoelectronic applications. In the fabrication of devices based on heterostructures, the interfacial band alignment is of significant interest. Investigation of heterojunction band discontinuities is important for device design because the valence and conduction band offsets determine the transport and confinement properties at the interface. A fundamental objective for technology and basic research would be the control of the band discontinuities.¹ The use of Si_3N_4 as a passivation layer on GaN-based high voltage devices and as a gate insulator in field effect transistor (FET) devices are potential applications that require knowledge of the band alignment of this interface.

Recent studies of the electrical properties of the $\text{Si}_3\text{N}_4/\text{GaN}$ interface by Arulkumaran *et al*² and Nakasaki *et al*³ have reported interface trap densities of $6.5 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ and $5.0 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ with clear deep depletion behavior. Chang *et al*⁴ found that silicon nitride passivation enhances light output and increases the reliability of GaN-based light emitting diodes by reducing the leakage current. Electrical data in the literature indicates the promise of advanced GaN metal-insulator-semiconductor (MIS) devices.²⁻⁴ While several groups have employed photoemission techniques to study GaN/metal interfaces,⁵⁻⁷ only Nakasaki *et al*³ report band offsets for GaN/ Si_3N_4 interfaces. They report type I band alignment with a valence band offset of 1.0-1.2 eV for the $\text{Si}_3\text{N}_4/\text{GaN}(0001)$ interface.

Application of the electron affinity model (EAM) is a first approach to characterizing the electronic properties of a heterostructure. This model holds in the case when there is no change in the potential at each surface as the interface is formed. An alternative approach is the

interface dipole model, where the structure of the interface causes a shift in the entire band lineup relative to the predictions of the EAM.

The main focus of our experiment is to measure the band offsets and to explore the interface dipole at the heterostructure interface. The combination of XPS and UPS measurements is a well-established method of determining band discontinuities at heterojunction interfaces.^{8,9} Our basic approach in this study is to obtain clean GaN surfaces through an ammonia exposure at elevated temperatures and to form an Si_3N_4 layer by depositing silicon on the clean surface followed by a low temperature ECR plasma nitridation. The XPS and UPS measurements are obtained after each step in the process, yielding the band bending from the shifts in the gallium 3d and 3p core levels. The band offsets and electron affinities are deduced from the UPS spectra, and the contribution of the interface dipole is determined from the XPS and UPS measurements.

II. Experimental Procedures

The GaN films used in this study were grown via metallorganic vapor phase epitaxy (MOVPE) on 50 mm diameter on-axis 6H (0001) substrates with a conducting AlN (0001) buffer layer. The thickness of the GaN epilayer and the AlN buffer were 1.1 μm and 0.1 μm , respectively. Silicon was used as the n-dopant, and magnesium was used as the p-dopant. Dopant concentrations ($N_d - N_a$) of $1 \times 10^{17} \text{ cm}^{-3}$ and ($N_a - N_d$) of $2 \times 10^{18} \text{ cm}^{-3}$ were measured for the n-type and p-type samples using capacitance-voltage measurements with a mercury probe.

Ex situ surface preparation consisted of a series of three sequential dips of 1 minute in trichloroethylene, acetone, and methanol, followed by an immersion in 49% HCl for 10 minutes.

The samples were then placed in the load lock for entry into the transfer line that interconnects several analysis and processing chambers. After the initial surface analysis, the sample was moved to the gas source molecular beam epitaxy chamber (GSMBE) for *in situ* cleaning. The *in situ* cleaning process consisted of annealing at 860°C for 15 minutes in an NH₃ atmosphere, where the details have been previously reported.^{5,10,11}

After cleaning and other process steps, the samples were transferred in UHV to the surface analysis chambers. For XPS, a dual anode source was used to generate magnesium (1253.6 eV) or aluminum (1486.6 eV) X-rays. The resolution of the analyzer was determined from the full width half maximum (FWHM) of a gold 4f_{7/2} spectral peak to be approximately 1.0 eV; however through curve fitting, spectral peak positions could be resolved to ± 0.1 eV.

UPS with He I (21.2 eV) radiation was employed to measure the electronic states near the valence band and to determine the electron affinity. A negative 4 V bias was applied to the sample to overcome the work function of the analyzer.

To form the silicon nitride layer, silicon was deposited via molecular beam epitaxy (MBE), and nitrided by an electron cyclotron resonance (ECR) N₂ plasma. The plasma conditions were 300 W of microwave power for 30 seconds, pressure of 7.5×10^{-4} Torr, and a sample temperature of 300°C.

The XPS and UPS spectra were measured to obtain information about the core levels and valence band after each of the following steps: 4Å Si deposition, N₂ plasma of the Si layer at 300°C, a 2Å Si deposition (6Å total) and N₂ plasma at 300°C, 650°C anneal for 15 minutes, a final 3Å Si deposition (9Å total) and N₂ plasma at 300°C, and a 15 minute 650°C final anneal. XPS allows chemical bonding and band bending to be discerned by following the relative peak position shift during the evolution of the experiment. Valence band information, as well as the

electron affinity of each material, are determined from the UPS spectra. A combination of XPS and UPS provides information about the band discontinuities at the interface, as well as allows an observation of a change in the interfacial dipole.

III. Results

The evolution of the UPS spectra from the clean GaN through nitridation and final anneal of the deposited 9Å Si for the n-type experiment is shown in Figure 1. The valence band maximum (VBM) of the clean GaN surface was determined from an extrapolation of a line fit to the leading edge of the spectrum. The VBM of the GaN and the Si₃N₄ signal were measured at 3.1 ± 0.1 eV and 2.3 ± 0.1 eV (referenced to the Fermi level), respectively. Because the deposited layers obscure the VBM, it is necessary to detect a more intense bulk GaN spectral feature to reference the position of the VBM. A feature at 13.4 eV in the spectra shown in Figure 1 has been attributed to a GaN bulk excitation.¹² This feature shifts to a lower binding energy by 0.2 ± 0.1 eV with the deposition of 4Å of Si and the nitridation that followed, and is ascribed to an increase of the band bending by 0.2 eV. Following the peak movement is only possible when the substrate emission is observable, therefore when the layer thickness obscures this emission, further information about band bending cannot be obtained. In our UPS measurements, emission from the substrate was not detected for the final 3Å (9Å total) silicon deposition and nitridation. With increased thickness, the valence band turn-on and signature peaks for Si₃N₄ remained unchanged.

The valence band turn-on was measured to be 1.4 ± 0.1 eV for the p-type GaN material. From the doping concentration of 2×10^{18} in the p-type GaN, the bulk Fermi level was determined

to be ~300 meV above the valence band maximum. This indicates significant downward band bending of 1.1 eV for the clean p-type GaN surface.

The electron affinity can be obtained from the UPS by determining the width of the spectra, using the relation:

$$\chi = h\nu - W - E_g \quad (1)$$

where W is the spectral width from the VBM to the low energy cut-off, $h\nu$ is the photon energy (21.2 eV), and E_g is the bandgap of the material. Using 3.4 eV as the bandgap, the electron affinity was determined to be 3.1 ± 0.1 eV for both the n- and p-type GaN. As a verification that our measured turn-on is indeed the VBM, we note that our results indicate that the Ga 3d is 17.7 eV below the VBM, which is consistent with Waldrop and Grant.¹³

The same approach is used to determine the electron affinity of the Si₃N₄ layer. Though the bandgap of Si₃N₄ has a range of reported values,^{14,15} we will use the value of 5.3 eV and consequently obtain an electron affinity of 1.8 ± 0.1 eV. While this value is similar to prior reports^{16,17} of 2.1 eV, the uncertainty of the bandgap of the material, as well as the ± 0.1 eV measurement uncertainty can account for the 0.3 eV deviation.

The evolution of the gallium 3d peak during the n-type GaN experiment is shown in Figure 3. The initial peak position for the clean surface was determined to be 20.63 ± 0.1 eV. Spectra observed after the Si deposition showed shifts that were smaller than 0.1 eV. For the final surface, which consisted of an accumulated 9 Å of Si, which was nitrided, the peak was observed at 20.43 ± 0.1 eV, indicating a shift of 0.2 ± 0.1 eV for the entire experiment. This shift is consistent with the movement of the bulk peak located at ~13.4 eV in the UPS spectra shown in Figure 1.

Figure 4 represents the evolution of the gallium 3p and silicon 2p core levels during the n-type experiment. The Ga 3p core levels are consistent with the Ga 3d core levels, shifting to a lower binding energy by 0.2 eV during the course of the experiment. This shift to a lower binding energy is ascribed to an increase in the band bending by 0.2 eV during interface formation. The Si 2p peak position after the initial deposition of Si is found to be 100.03 ± 0.1 eV. After nitridation, this core level shifts to a peak position of 102.44 ± 0.1 eV, remaining essentially constant throughout the remainder of the experiment. This large 2.44 eV shift of the Si 2p core level is indicative of a chemical shift due to the Si-N bonding, and is consistent with reported values for Si_3N_4 .^{18,19} In an additional approach to explore the composition of our films, we measured the energy difference between the N 1s and Si 2p core levels. For the thin films in this study the N 1s core level was obtained, but the Si-N peak was not resolvable due to the dominance of the nearby Ga-N peak. We prepared thicker films of Si_3N_4 on GaN using the same techniques, as well as thin films on silicon. In both cases, the energy difference between the N 1s and Si 2p core levels was found to be 295.65 ± 0.1 eV. Literature values for this difference are found to be 295.7 eV for Si_3N_4 films, while for SiN_x ($x < 1.33$) films a value of 295.4 eV is observed.^{19,21} Moreover, analysis of the integrated areas for the N 1s and Si 2p core level peak yielded a N/Si ratio of 1.32 ± 0.01 . These results are consistent with the formation of stoichiometric Si_3N_4 .

The evolution of the gallium 3d peak for the p-type GaN experiment was also measured. The initial peak position for the clean surface was observed at 18.88 ± 0.1 eV. After the 4 Å Si deposition and nitridation, the peak shifted to a value of 19.38 ± 0.1 eV, a difference of ~ 0.5 eV. After each process with a 650 °C, the Ga 3d core level shifted from the value of the as deposited film by an additional ~ 0.2 eV, as evidenced by the peak positions of the Si_3N_4 formed from 6 Å

total Si and plasma/650 °C anneal and the 9 Å total Si and plasma/650 °C anneal treatments shown at 19.61 ± 0.1 eV and 19.58 ± 0.1 eV, respectively. The purpose of the anneal is to allow reconstruction and densification of the nitride film after deposition, therefore, improving the quality of the film for device fabrication.^{22,23} During the course of the experiment we observed a shift in the Ga 3d peak of 0.70 ± 0.1 eV. This shift is consistent with the gallium 3p core level, suggesting that the change in the core level is due to a change in the band bending.

IV. Discussion

The method used for determining the valence band offset is similar to that of Waldrop and Grant and Kraut *et al.*²⁴ Their basic approach is to reference the VBM to a core level in the XPS spectra for each semiconductor and to use the measured difference between the core level energies to discern the band discontinuities. In our study, we use UPS to measure the energy of the VBM relative to the Fermi level, and XPS is used to obtain band bending information by measuring the shift in the core level energies relative to the Fermi level. A combination of these two photoemission techniques provides the band alignment at the heterojunction interface.

Figure 5 shows the proposed band lineups for the n-type GaN/Si₃N₄ interface. The VBO determination is the measured UPS turn-on for GaN (3.1 eV), minus the Si₃N₄ turn-on (2.3 eV), minus the band bending (0.2 eV). This value, along with knowledge of the bandgap of the material, allows the CBO to be deduced. The VBO is found to be type II band alignment, where the valence band of the Si₃N₄ is 0.6 ± 0.1 eV above the GaN VBM, and the CBO is 2.5 eV.

Figure 6 shows the proposed band lineups for the p-type GaN/Si₃N₄ interface. The UPS turn-on for the clean GaN and the Si₃N₄ was observed at 1.4 eV and 2.2 eV, respectively. XPS spectra

showed downward band bending of ~ 0.8 eV during formation of the interface. The VBO is again found to be type II band alignment 0.4 ± 0.1 eV above the GaN VBM, and the CBO is 2.3 eV.

The measured electron affinities for GaN and Si_3N_4 are represented in Figures 5 and 6. The electron affinity model of heterojunction formation assumes that the vacuum levels would align at the interface. Our results show a deviation from the EAM of 1.2 eV and 1.0 eV for the n-type GaN and p-type GaN substrates, respectively. The EAM model is based on the premise that the interface is formed without disruption of the surface electronic states of either of the two materials. The measured difference between the prediction of the EAM and the experimentally observed band offset represents a change in the interface dipole.

As an alternative to the electron affinity model, it may be considered that the heterojunction band offsets are determined by alignment of the charge neutrality levels (CNL) of the two materials. The charge neutrality levels represent the branch point of the surface (or interface) states as they are related to the valence or conduction band. Charge can transfer between the interface states of the two materials, which will cause an interface dipole. The band offset will be determined by the relative position of the CNL of the two materials if the density of states is high or if the CNL of the two semiconductors are similar in relative energy.

Robertson¹⁶ adapted the Schottky barrier interface defect model presented by Cowley and Sze²⁵ to employ the CNL as the pinning levels at a heterojunction interface. This model was used to analyze silicon/oxide interfaces, and the model seems consistent with most experimental results. This model is given by the relation:

$$\phi_{CBO} = (\phi_{CNL,a} - \phi_{CNL,b}) - (E_{g,a} - E_{g,b}) + S\{(\chi_a - \chi_b) + (E_{g,a} - E_{g,b}) - (\phi_{CNL,a} - \phi_{CNL,b})\} \quad (2)$$

Where ϕ_{CBO} is the CBO, χ and ϕ_{CNL} are the electron affinities and charge neutrality levels for each semiconductor (a and b), and S is a pinning factor based on the dielectric properties of the

materials. Here, the ϕ_{CNL} are defined relative to the VBM of each semiconductor. A value of $S=1$ represents the EAM while a value of 0 represents pinning at the CNL levels. To our knowledge, the CNL of Si_3N_4 has not been reported. Using the value of S for the Si_3N_4 -Si interface (0.51) and the measured band offset from previous work,^{16, 23} we can deduce the CNL of Si_3N_4 to be 1.5eV above the valence band maximum. While more research is necessary to assign a CNL value for Si_3N_4 , it is reasonable to consider this prediction of the valence band offset for comparison to our experimental results. Monch²⁶ has reported the CNL of GaN to be 2.37 eV above the valence band maximum. Though the dielectric screening parameter S has not been determined for the GaN/ Si_3N_4 interface, in the limits of $S=0$ and $S=1$ the valence band types and offsets would be type II 0.9 eV and type I 0.9eV, respectively. If the assumption is made that the parameter S is similar to that for the Si/ Si_3N_4 interface (0.51), the CNL relation given in Eq. 2 predicts the valence band offset to be $\sim 0.1\text{eV}$ (essentially no offset) for the GaN/ Si_3N_4 interface. Conversely, the dielectric screening parameter can be deduced for the interface using our results and the CNL of GaN and Si_3N_4 . A value of $S=0.26$ is obtained for the GaN/ Si_3N_4 interface.

This prediction, as well as our results, are significantly different from the results by Nakasaki *et al.*,³ who report type I band alignment with an offset of 1.0-1.2eV for the GaN/ Si_3N_4 interface. A factor that could play a major role in this difference is the cleaning method used for the GaN. Their studies used an NH_4OH etch and a combination of H_2 and N_2 plasmas for *in situ* surface preparation. While the oxygen content was greatly reduced from the as-loaded case, a significant amount remained after surface preparation, suggesting Ga-O bonding.³ In a previous study¹⁰, the GaN/ SiO_2 interface was examined via photoemission, showing a type I alignment and a VBO $\sim 2\text{ eV}$. We suggested that Ga-O bonding exists at the GaN/ SiO_2 interface and

contributes to the large offset and interfacial dipole change. Our study begins with a clean GaN surface (contamination levels of <1% for oxygen and carbon) that allows the GaN/Si₃N₄ interface to be measured more precisely.

In an attempt to understand the relation of our measured band alignment and the different models for heterostructure band alignment, in Figure 7 we have compared our measured interface alignments to experimental results for Si₃N₄ on Si.^{16,22,23} In both cases the diagrams are aligned to the vacuum level at the Si₃N₄, which has been measured to be at the same energy relative to the silicon nitride bands. The bandgap of each material is indicated, as is the VBO. The position of the vacuum level of the clean semiconductor surface is indicated, and the difference between these values and the surface vacuum level is the deviation from the EAM. This difference represents the change in the interface dipole, and was found to be 0.5 and 1.2 eV for Si₃N₄ on Si and GaN, respectively.

Also indicated in Figure 7 is the CNL of the semiconductors.^{16,26} Additionally, the predicted CNL of Si₃N₄ (1.5 eV) deduced as described above is also represented. We observe that the CNL's nearly align for the GaN/Si₃N₄ interface, suggesting the correlation of this interface with the CNL model with a low dielectric screening parameter S . The progression of the interface dipole deduced from the deviation from the EAM is most likely related to the changes at the semiconductor surface since the silicon nitride is the same in both cases. For the Si/Si₃N₄ interface, the Si surface reconstruction is expected to change during the formation of the nitride layer. This effect alone could account for the small change in the interface dipole, and the same could be true for the GaN/Si₃N₄ interface. For GaN/Si₃N₄, we expect Ga-N-Si bonding to exist within the first few monolayers at the heterojunction interface. Because of the similarity in bonding at the interface we may expect a smaller interface dipole than that of the GaN/SiO₂

interface. Indeed, this is the case where we find an 1.1 ± 0.1 eV interface dipole for GaN/Si₃N₄ and a 1.7 ± 0.1 eV for the GaN/SiO₂ interface.

V. Conclusions

The surface and interface properties of n- and p-type GaN/Si₃N₄ were systematically investigated by photoemission techniques and band alignment information was obtained. Annealing in ammonia at 860°C provided clean stoichiometric GaN surfaces with ~ 0.2 eV upward band bending and ~ 1.1 eV downward band bending for the n-type and p-type surfaces, both with an electron affinity of 3.1 eV. For GaN/Si₃N₄, type II band alignment was observed and valence band offsets were measured to be ~ 0.5 eV for both the n-type and p-type cases. The interface dipole deduced from comparison with the electron affinity model was 1.1 ± 0.1 eV. The charge neutrality model provided a reasonable description of the band alignment of the GaN/Si₃N₄ interface. It is suggested that the presence of oxygen at the interface could substantially change the band offsets. These results indicate that Si₃N₄ should passivate n-type surfaces, but may not be appropriate for passivation of p-type surfaces.

Acknowledgements

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FIGURE CAPTIONS

Figure 1. UPS Spectra of the valence band maximum of: a) CVC clean n-GaN, b) 4Å Si, c) 4Å Si and N₂ plasma, d) 6Å Si and N₂ plasma, e) 6Å Si, N₂ plasma and 650°C anneal, f) 9Å Si and N₂ plasma, g) 650°C anneal.

Figure 2. UPS spectra of the valence band maximum of CVC clean n-type GaN and the Si₃N₄ final surface, with the valence band maximum indicated by dashed lines.

Figure 3. XPS Ga 3d core level spectra of : a) CVC clean n-GaN, b) 4Å Si, c) 4Å Si and N₂ plasma, d) 6Å Si and N₂ plasma, e) 6Å Si, N₂ plasma and 650°C anneal, f) 9Å Si and N₂ plasma, g) 650°C anneal. The peak positions of the initial surface, as well as the final surface are indicated with dashed lines.

Figure 4. XPS Ga 3p and Si 2p core level spectra of : a) CVC clean n-GaN, b) 4Å Si, c) 4Å Si and N₂ plasma, d) 6Å Si and N₂ plasma, e) 6Å Si, N₂ plasma and 650°C anneal, f) 9Å Si and N₂ plasma, g) 650°C anneal. The peak position of the Si 2p core level after silicon deposition, as well as the final surface are indicated with dashed lines.

Figure 5. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and SiO₂. The valence band offset, E_v , conduction band offset, E_c , band bending, and interface dipole, Δ , are represented.

Figure 6. Deduced bands for the clean p-type GaN surface (left) and the interface between p-type GaN and SiO₂. The valence band offset, E_v , conduction band offset, E_c , band bending, and interface dipole, Δ , are represented.

Figure 7. Band alignment of Si/Si₃N₄ and GaN/Si₃N₄ interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the Si₃N₄ surface, which is common in both interfaces. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap. The VBO are determined from the measurements.

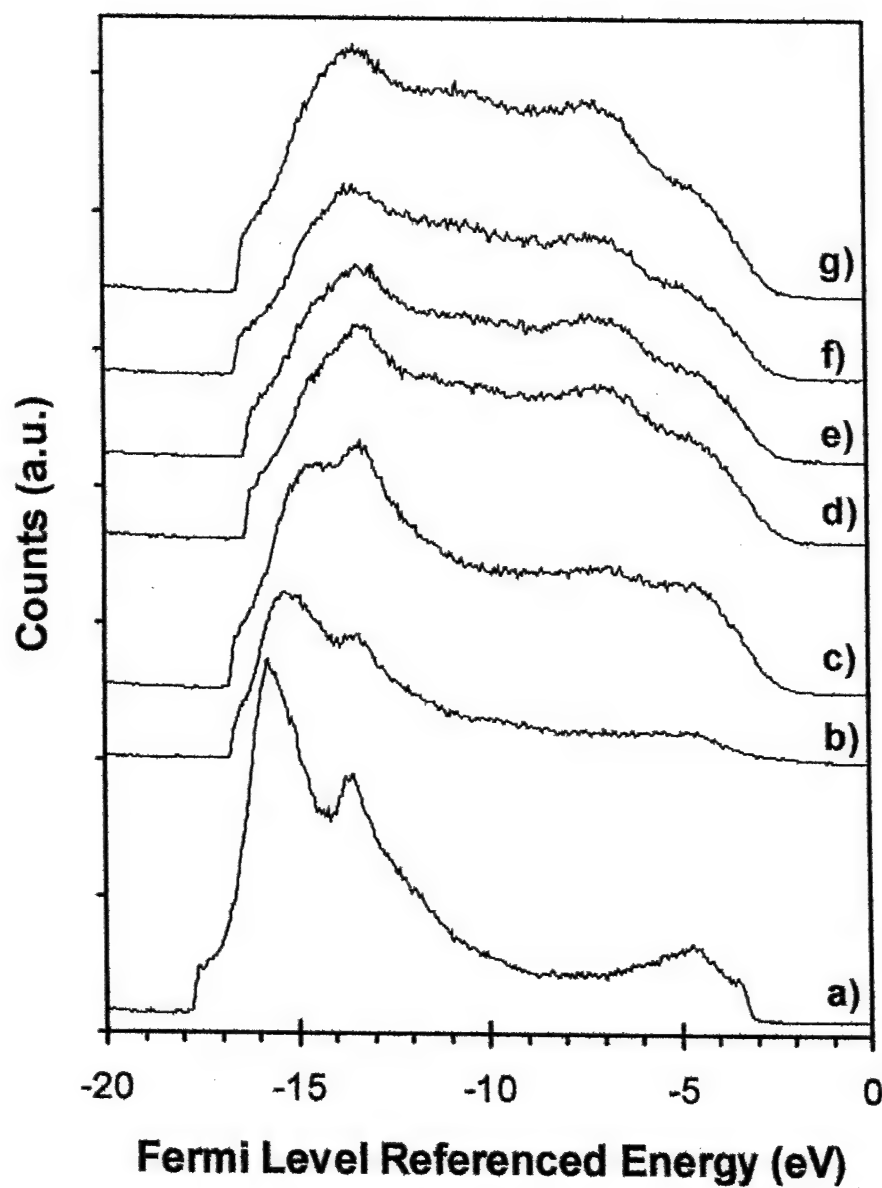


Figure 1. UPS Spectra of the valence band maximum of: a) CVC clean n-GaN, b) 4 Å Si, c) 4 Å Si and N₂ plasma, d) 6 Å Si and N₂ plasma, e) 6 Å Si, N₂ plasma and 650°C anneal, f) 9 Å Si and N₂ plasma, g) 650°C anneal.

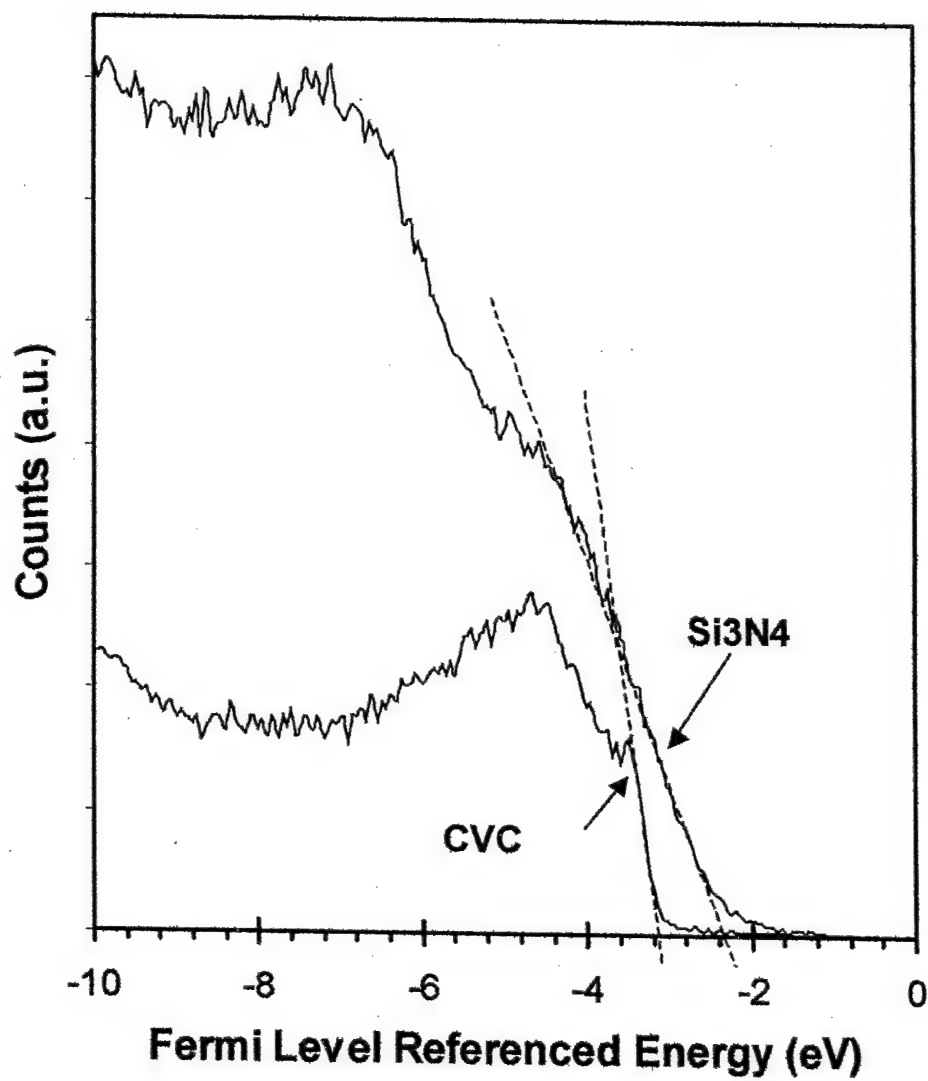


Figure 2. UPS spectra of the Valence Band turn-on of clean GaN and the Si_3N_4 final surface

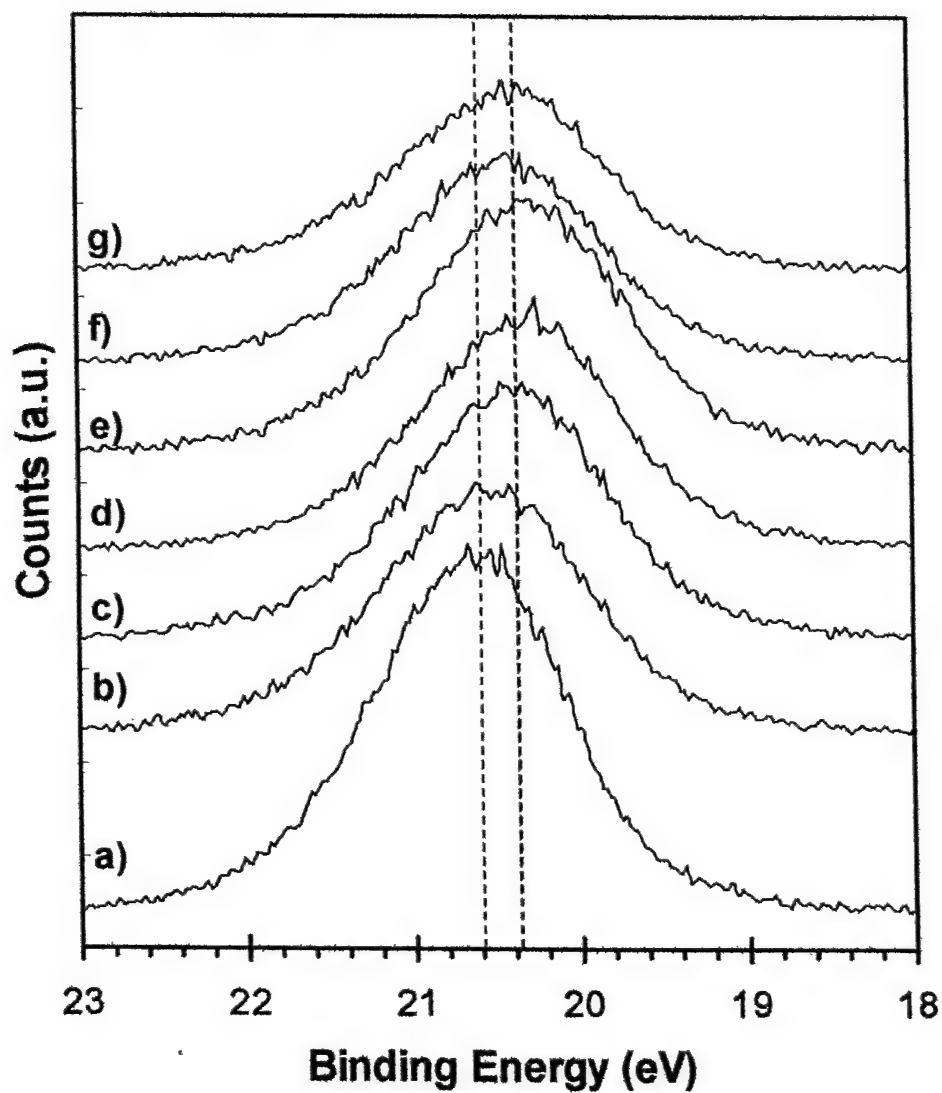


Figure 3. XPS Ga 3d core level spectra of : a) CVC clean n-GaN, b) 4 Å Si, c) 4 Å Si and N₂ plasma, d) 6 Å Si and N₂ plasma, e) 6 Å Si, N₂ plasma and 650°C anneal, f) 9 Å Si and N₂ plasma, g) 650°C anneal. The peak positions of the initial surface, as well as the final surface are indicated with dashed lines.

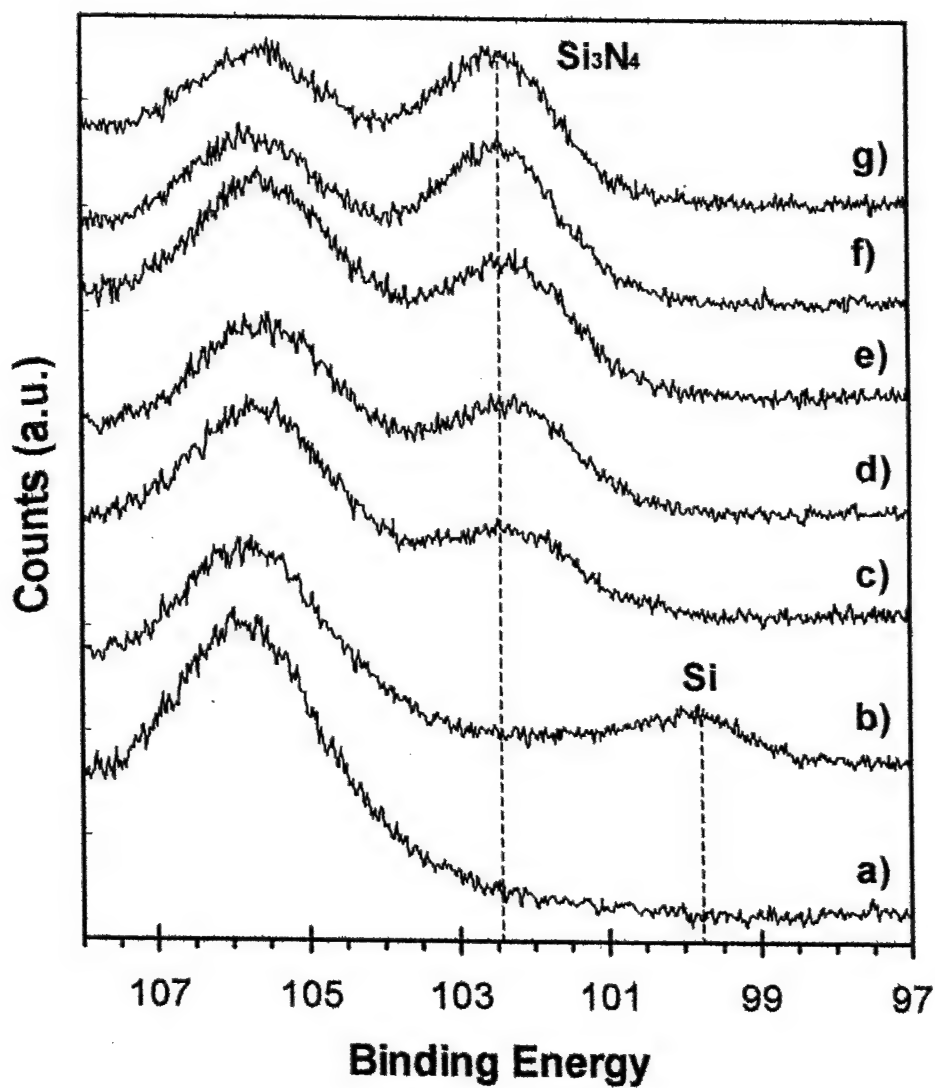


Figure 4. XPS Ga 3p and Si 2p core level spectra of : a) CVC clean n-GaN, b) 4Å Si, c) 4Å Si and N₂ plasma, d) 6Å Si and N₂ plasma, e) 6Å Si, N₂ plasma and 650°C anneal, f) 9Å Si and N₂ plasma, g) 650°C anneal. The peak position of the Si 2p core level after silicon deposition, as well as the final surface are indicated with dashed lines.

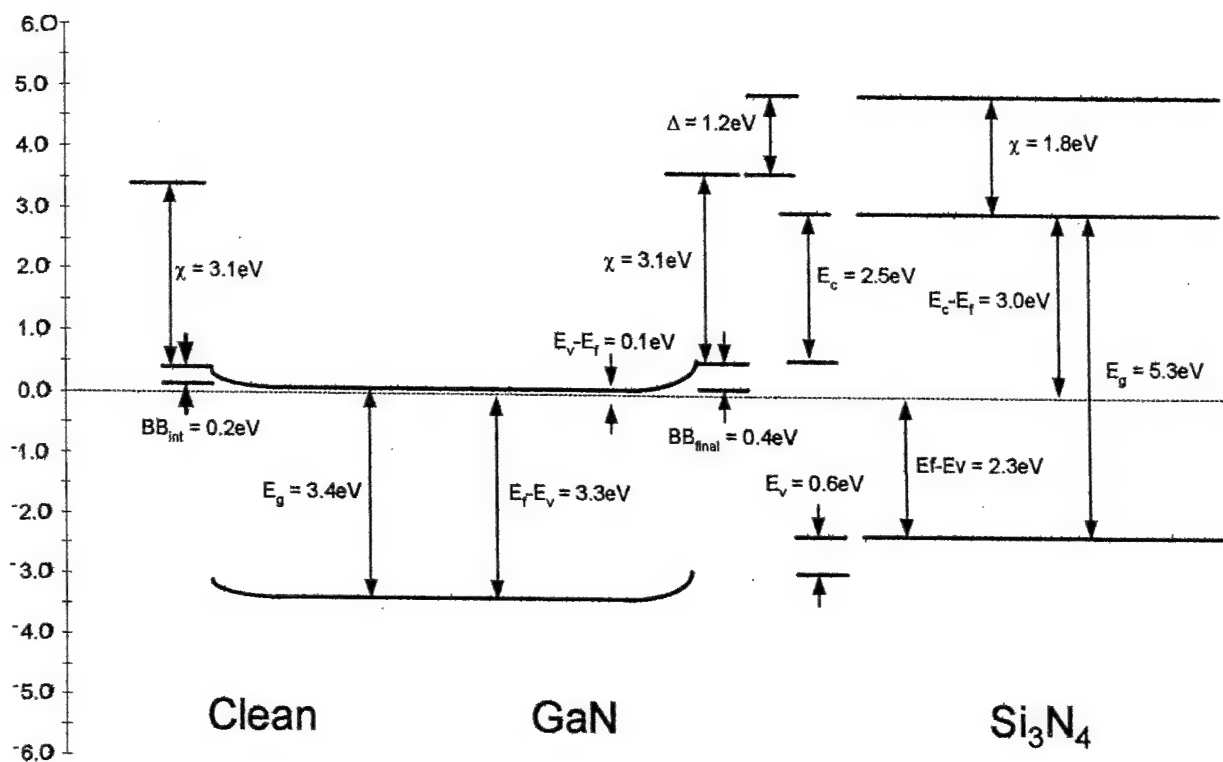


Figure 5. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and SiO_2 . The valence band offset, E_v , conduction band offset, E_c , band bending, and interface dipole, Δ , are represented.

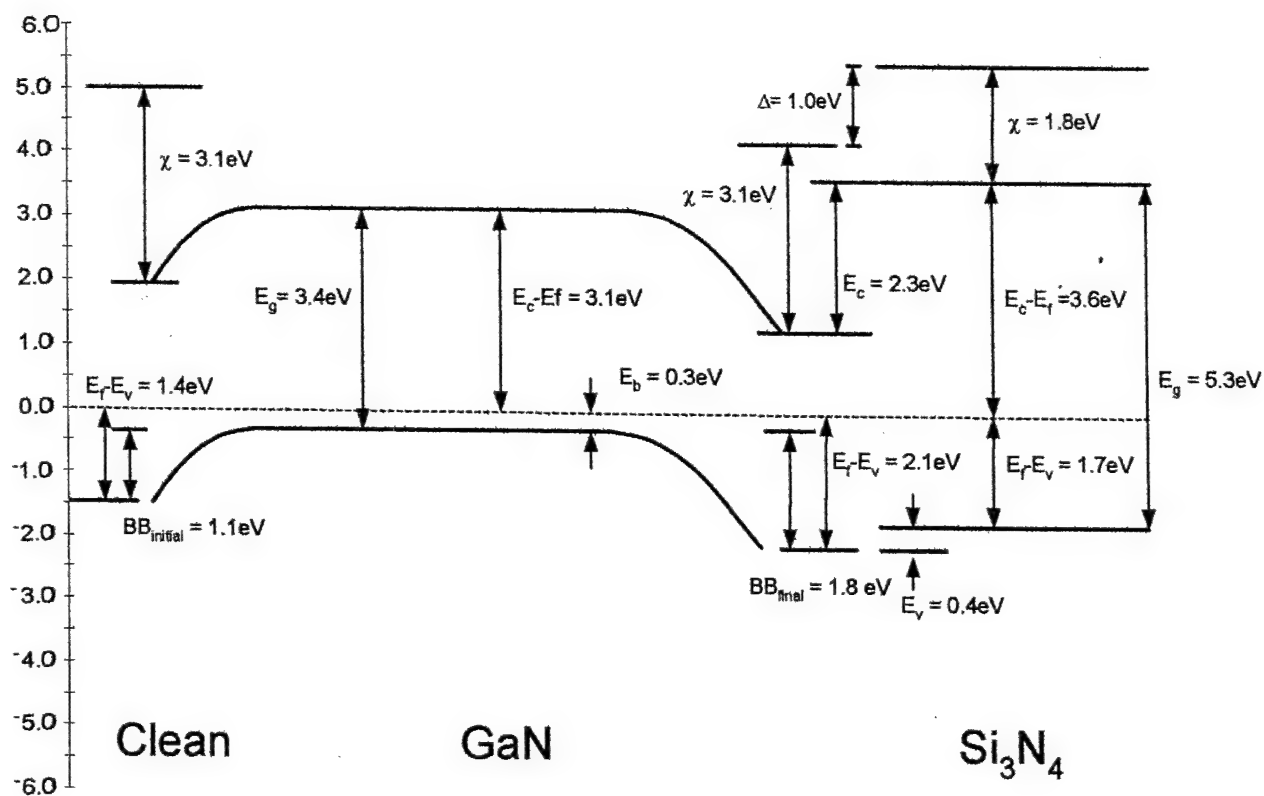


Figure 6. Deduced bands for the clean p-type GaN surface (left) and the interface between p-type GaN and SiO_2 . The valence band offset, E_v , conduction band offset, E_c , band bending, and interface dipole, Δ , are represented.

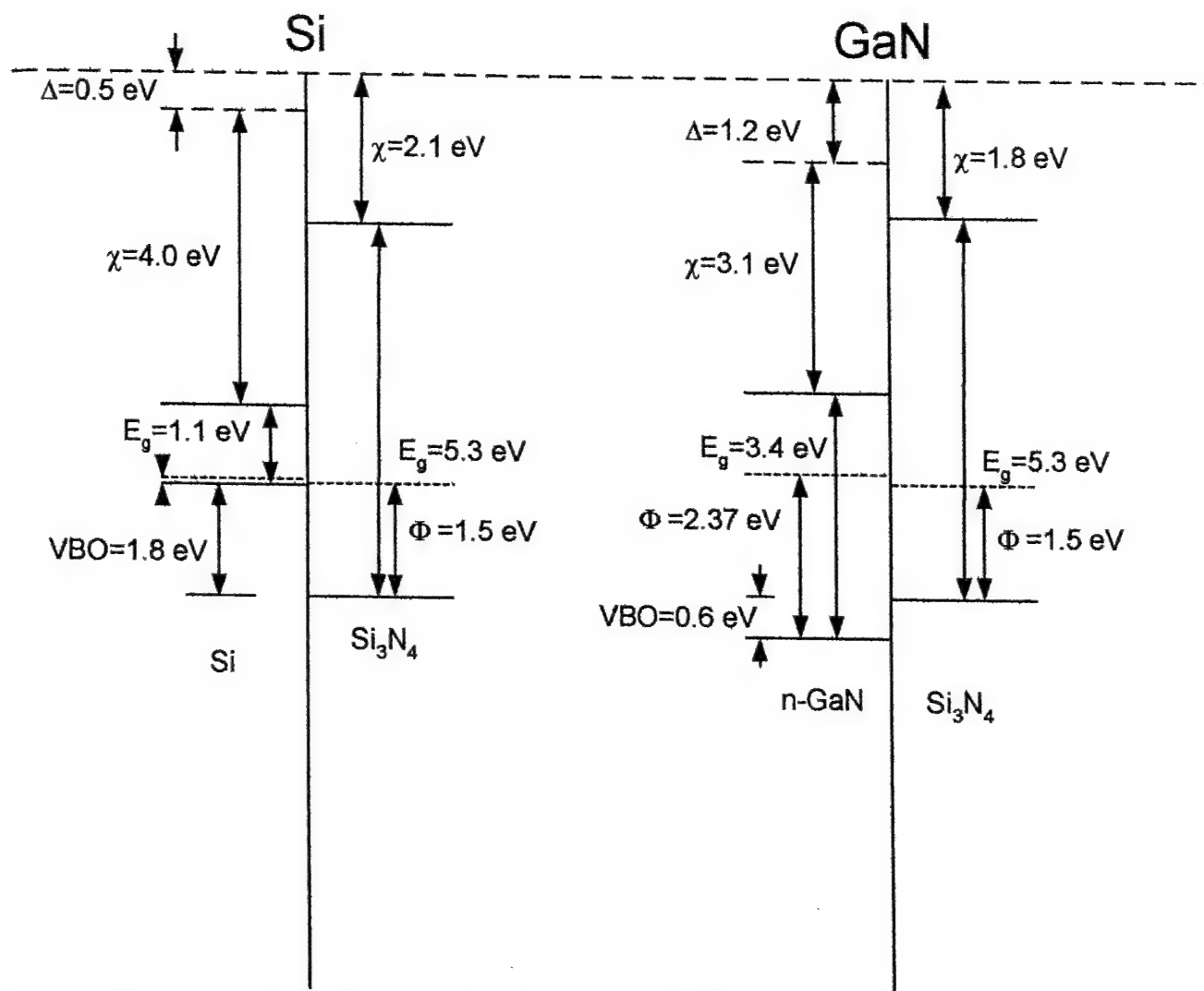


Figure 7. Band alignment of Si/Si₃N₄ and GaN/Si₃N₄ interfaces. The dashed line at the top of the figure corresponds to the electron affinity of the Si₃N₄ surface, which is common in both interfaces. The deviation from the electron affinity model is shown as Δ , and the charge neutrality level (CNL) is indicated as a dashed line within the band gap. The VBO are determined from the measurements.

Band offset measurements of the GaN(0001)/HfO₂ interface

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ABSTRACT

Photoemission spectroscopy has been used to observe the interface electronic states as HfO₂ was deposited on clean n-type Ga-face GaN (0001) surfaces. The HfO₂ was formed by repeated deposition of several monolayers of Hf followed by remote plasma oxidation at 300 °C, and a 650 °C densification anneal. The 650 °C anneal resulted in a 0.6 and 0.4 eV change in band bending and valence band offset, respectively. The final annealed GaN/HfO₂ interface exhibited a valence band offset of 0.3 eV and a conduction band offset of 2.1 eV. A 2.0 eV deviation was found from the electron affinity band offset model.

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Properties such as high dielectric constant, low leakage current, and relatively low interface density suggest the promise of HfO_2 in electronic device fabrication. The large band gap of 5.8 eV would be consistent with applications on wide band gap semiconductors such as GaN. The use of HfO_2 and other high- κ dielectrics as a passivation layer on GaN-based high voltage devices and as a gate insulator in field effect transistor (FET) devices requires knowledge of the band alignment of this interface.

In our study, HfO_2 films are formed on clean GaN (0001) surfaces prepared by an in situ ammonia exposure at an elevated temperature.¹ While several studies^{2,3} have employed photoemission techniques to explore the Si- HfO_2 interface, there has been, to our knowledge, no similar report for the GaN- HfO_2 interface.

A first approach to describing a heterostructure interface is to apply the electron affinity model (EAM). This model holds in an ideal case, where there is no potential created as the heterostructure is formed. Alternatively, a deviation from the EAM can be represented as a change in the interface dipole. Tersoff⁴ suggested that the band alignment between two semiconductors is controlled by the charge transfer across the interface and the resulting interface dipole in a fashion similar to Schottky barrier models. Recently, Robertson⁵ employed charge neutrality levels (CNL) and dielectric screening to relate the relative contribution of the electron affinity model and the interface dipole in determining the band offset of oxides on Si.

The focus of our experiment is to use photoemission to measure the band offsets of HfO_2 on clean GaN (0001) and to compare the results to the EAM. The deviation will be discussed in terms of a change in the interface dipole.

The GaN films were grown via metallorganic chemical vapor deposition (MOCVD) on 50 mm diameter on-axis Si-face, 6H SiC (0001) substrates with a conducting AlN (0001) buffer

layer. The thickness of the GaN epilayer and the AlN buffer were 1.1 μm and 0.1 μm , respectively. Prior research has established that MOCVD growth of GaN on Si face SiC (0001) results in Ga face GaN (0001).^{6,7} Silicon was used as the n-dopant with a net donor concentration ($N_d - N_a$) of $1 \times 10^{17} \text{ cm}^{-3}$ determined by mercury probe capacitance-voltage measurements.

The in situ surface cleaning and the experimental procedures are essentially identical to those described in a previous study.⁸ X-ray photoemission spectra (XPS) and UV photoemission spectra (UPS) were obtained after each process step in a sequence of experiments. Shifts of the XPS peaks and the evolution of the valence band spectra were recorded. The spectra were measured after each of the following steps: a 4 \AA Hf deposition, O_2 plasma at 300°C, 4 \AA Hf (8 \AA total Hf) and O_2 plasma at 300°C, 650°C anneal for 15 minutes, a final 4 \AA Hf deposition (12 \AA Hf total) and O_2 plasma at 300°C, and a 15 minute 650°C final anneal. For the 12 \AA Hf total, the ultimate thickness of the HfO_2 film was calculated to be $\sim 20 \text{ \AA}$ based on bulk densities. The attenuation of the GaN XPS core levels was consistent with this value.

The evolution of the UPS spectra from the clean GaN through the oxidation and anneal of the 12 \AA Hf is shown in Figure 1. The VBM of the clean GaN surface was determined from an extrapolation of a line fit to the leading edge of the spectrum and was measured to be at $3.0 \pm 0.1 \text{ eV}$ (referenced to the Fermi level). As a verification that our measured turn-on is indeed the VBM, we note that our results indicate that the Ga 3d is 17.7 eV below the VBM, which is consistent with the careful study by Waldrop and Grant.⁹ The electron affinity of the GaN and the HfO_2 were deduced from the UPS using the relation $\chi = h\nu - W - E_g$ where W is the spectral width from the VBM to the low energy cut-off, $h\nu$ is the photon energy (21.2 eV), and E_g is the bandgap of the material. For the clean n-type GaN surface, the width of the UPS spectrum was

measured to be 14.8 eV, and using 3.4 eV as GaN bandgap, we find an electron affinity of 3.0 eV, which is in agreement with prior reports.^{10,11} Similarly, the turn-on for the HfO₂ is observed at ~3.3 eV below the Fermi level, and the spectral width is measured to be 12.5 eV. Assuming a bandgap of 5.8 eV, we obtain an electron affinity of 2.9 eV, which is within the experimental error of the estimated value reported by Robertson.⁵

The evolution of the Ga 3d, Ga 3p_{3/2}, N 1s, Hf 4f and O 1s core levels are summarized in Table 1. The core level spectra indicate two significant effects. The first is the level of band bending in the GaN. Here, it is found that both the clean surface and the annealed HfO₂/GaN interface exhibited 0.3 eV upward band bending. The second effect is that we find a ~0.9 eV shift of the O 1s and Hf 4f core levels upon annealing to 650°C. The evolution of the O 1s core level is displayed in Fig. 2. This shift is attributed to combined changes in band bending and band offset.

The method for determining the valence band offset is similar to that of Waldrop and Grant⁹ and Kraut *et al.*¹² Their basic approach is to reference the VBM to a core level in the XPS spectra for each semiconductor and to use the measured difference between the core level energies to discern the band discontinuities. In our study, we have employed UPS to measure the energy of the VBM, and XPS to measure core level energies. We can then express the VBO (ϕ_{VBO}) as

$$\phi_{VBO} = E_{VBM}^f - E_{VBM}^i + E_d \quad (1)$$

$$E_d = E_c^i - E_c^f$$

where E_{VBM}^i and E_{VBM}^f are the measured VBM of the initial clean GaN and the oxide grown on GaN, respectively, and E_d is the change in band bending as defined from the shift of the Ga or N

core levels. Here, E_c^i and E_c^f are the values of the core level of the initial clean surface and the deposited oxide surface, respectively. An increase in upward band bending is defined as positive.

Figure 3 displays the deduced band lineup for the as-deposited GaN-HfO₂ interface. The upward band bending of the clean surface increases by 0.6 eV as the interface is formed. The valence band offset is then the measured UPS turn-on for the HfO₂ on the GaN (2.3 eV), minus the GaN turn-on (3.0 eV), plus the increase in upward band bending (0.6 eV), resulting in a value of -0.1 eV. With this value and the knowledge of the bandgap of the material, the conduction band offset is obtained. The bandgap of HfO₂ has been reported to be 5.7-6.0 eV.^{2,5} A value of 5.8 eV was used for our conduction band offset and electron affinity calculations. The valence band offset is deduced to be -0.1 eV, and the conduction band offset is 2.5 eV for our as-deposited GaN/HfO₂ interface. This interface represents type II band alignment where the valence band maximum of the GaN lies below that of HfO₂ valence band.

Figure 4 shows the proposed band lineup for the n-type GaN-HfO₂ interface after annealing at 650 °C. The upward band bending is essentially the same as that of the clean surface. The valence band offset determination is then the measured UPS turn-on for the HfO₂ on the GaN (3.3 eV), minus the GaN turn-on (3.0 eV). The valence band offset is deduced to be 0.3 eV, and the conduction band offset is 2.1 eV.

The Ga face GaN (0001) is a polar surface, and the spontaneous polarization will lead to a negative bound charge at the GaN film surface. The polarization bound charge screened by the ionized donors would lead to upward band bending at the GaN surface, consistent with our observations of the clean surface. It is possible that some changes in the band bending observed during formation of the oxide are due to compensation or screening of the polarization surface bound charge. But the measurements of the band offsets will not be affected by these changes.

Our results indicate a deviation from the electron affinity model of 2.0 eV for the before and after annealing cases of the GaN-HfO₂ interface. As an alternative to the electron affinity

model, it has been proposed that heterojunction band alignments are determined by alignment of the charge neutrality levels (CNL) of the two materials. The charge neutrality levels represent the branch point of the surface or interface states related to the valence or conduction band. The presumption is that charge can transfer between the interface states of the two materials, which will cause an interface dipole. If the density of interface states is high, then the band offset will be determined by the relative position of the CNL of the two materials.

Recently, Robertson⁵ adapted the Schottky barrier interface defect model presented by Cowley and Sze¹³ to employ the CNL as the pinning levels for heterojunction interfaces. The model was applied to analyze the band alignment of a range of oxides on silicon, and the model seems consistent with most experimental results. In this model, the band lineup is described by the relation:

$$\phi_{CBO} = (\phi_{CNL,a} - \phi_{CNL,b}) - (E_{g,a} - E_{g,b}) + S\{(\chi_a - \chi_b) + (E_{g,a} - E_{g,b}) - (\phi_{CNL,a} - \phi_{CNL,b})\} \quad (2)$$

Where ϕ_{CBO} is the CBO, χ and ϕ_{CNL} are the electron affinities and charge neutrality levels for each semiconductor (a and b), and S is a pinning factor based on the dielectric properties of the materials. Here, the ϕ_{CNL} are defined relative to the VBM of each semiconductor. A value of $S=1$ represents the EAM while a value of 0 represents pinning at the CNL levels.

Our measured electron affinities are 3.0 and 2.9 eV for the GaN and HfO₂, respectively. Robertson⁵ has reported the CNL of HfO₂ to be 3.7 eV, and the CNL of GaN has been assigned as 2.37 eV.¹⁴ Thus the EAM would predict a VBO of 2.3 eV and CBO of 0.1 eV. In the limit of strong pinning at the CNL, the model would predict a VBO of 1.3 eV and a CBO of 1.1 eV. It is evident that the observed VBO falls outside of the range that can be explained with the model (i.e. VBO between 1.3 and 2.3 eV) and the noted values of the CNL of GaN and HfO₂.

The instability observed after annealing at 650 °C is noteworthy. The results indicate a change in the interface dipole and an increase in upward band bending. We suggest that these effects may be due to excess O atoms in a negative ion state that have diffused towards the interface. The negative ions would form from charge from the GaN conduction band, which would result in upward band bending and an interface dipole that would lower the electronic bands of the oxide with respect to the GaN. Based on the 0.6 eV change in band bending and the GaN doping level, we estimate an excess charge of $\sim 3 \times 10^{11} \text{ e/cm}^2$.

In summary, the band alignment of an HfO₂ layer on n-type GaN has been investigated. The electron affinities for the clean n-type GaN and HfO₂ were measured to be 3.0 and 2.9 eV, respectively. After careful formation of the GaN-HfO₂ interface, upward band bending of 0.3 and 0.9 ± 0.1 eV existed for the as-grown and annealed interface, respectively. A valence band offset of -0.1 ± 0.1 eV (type II) was obtained for the as-grown interface, with a conduction band offset of 1.8 ± 0.1 eV (assuming $E_{\text{g HfO}_2} = 5.8$ eV). For the annealed interface, a valence band offset of 0.3 ± 0.1 eV was obtained, while the conduction band offset was determined to be 2.1 ± 0.1 eV. This result suggests the thermal stability of the hafnium oxide film significantly affects the electronic properties at the GaN-HfO₂ interface. An interface dipole of 2.0 eV was deduced from comparison with the electron affinity model for both the before and after annealing cases of the GaN-HfO₂ interface. Moreover, the charge neutrality model does not accurately predict the band alignment of the GaN-HfO₂ interface.

Acknowledgements

We gratefully acknowledge M. Park and B.J. Rodriguez for helpful discussions and piezoelectric calculations. This research was supported by the Office of Naval Research (MURI Project N00014-98-1-0654) and the Air Force Office of Scientific Research (grant F49620-00-1-0253.)

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Table I. XPS core level curve fitting results for the Ga 3p_{3/2}, Hf 4f, O 1s, Ga 3d, and N 1s energy levels. (Oxygen plasma is represented as O-Pl)

Process Step	Ga 3d		Ga 3p _{3/2}		N 1s		Hf 4f		O 1s	
	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)	Center (eV)	FWHM (eV)
CVC	20.6	1.6	105.8	2.7	398.0	1.7	-	-	-	-
4Å Hf	20.3	2.0	105.5	3.2	397.5	2.0	17.4	2.0	-	-
O-Pl	20.1	1.7	105.2	3.3	397.3	2.4	18.4	1.7	529.9	2.1
8Å Hf, O-Pl, anneal	20.7	1.5	105.8	3.1	397.9	1.6	19.2	1.5	530.8	1.9
12Å Si, O-Pl	20.1	1.6	105.2	3.3	397.4	2.4	18.3	1.6	529.9	2.2
Final	20.7	1.4	105.8	3.1	397.9	1.7	19.1	1.4	530.7	1.9

FIGURE CAPTIONS

1. UPS spectra of the valence band maximum of: a) CVC clean n-GaN, b) 4 Å Hf, c) 4 Å Hf and O₂ plasma, d) 8 Å Hf and O₂ plasma, e) 8 Å Hf, O₂ plasma and 650°C anneal, f) 12 Å Hf and O₂ plasma, g) 650°C anneal.
2. Oxygen 1s XPS spectra for: a) CVC Clean n-GaN, b) 4 Å Hf deposition, c) 4 Å Hf and O₂ plasma, d) 8 Å Hf, O₂ plasma, and 650°C anneal, e) 12 Å Hf and O₂ plasma, h) 650°C final anneal. The peak positions of the initial surface, as well as the final surface are indicated with dashed lines.
3. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and HfO₂ before annealing. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.
4. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and HfO₂ after annealing at 650 °C. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.

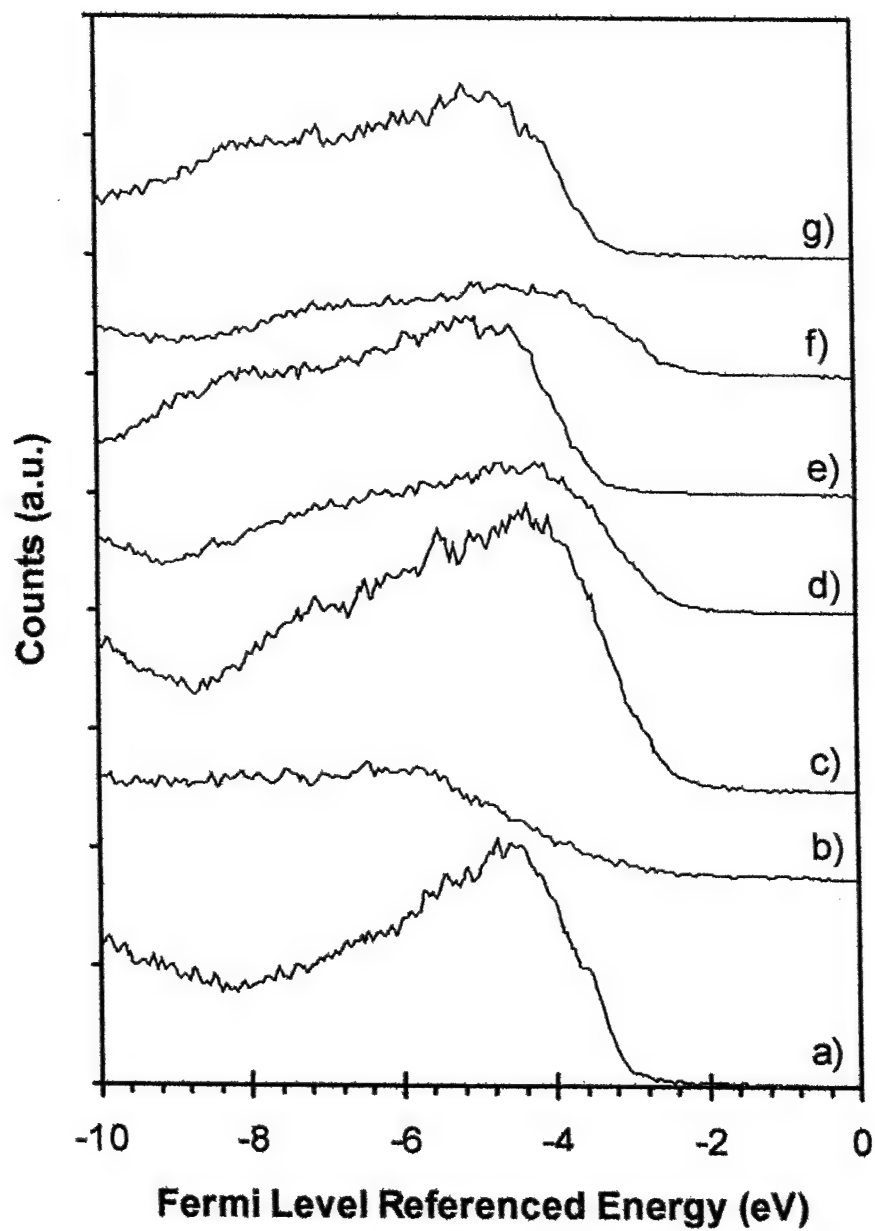


Figure 1. UPS spectra of the valence band maximum of: a) CVC clean n-GaN, b) 4 Å Hf, c) 4 Å Hf and O₂ plasma, d) 8 Å Hf and O₂ plasma, e) 8 Å Hf, O₂ plasma and 650°C anneal, f) 12 Å Hf and O₂ plasma, g) 650°C anneal.

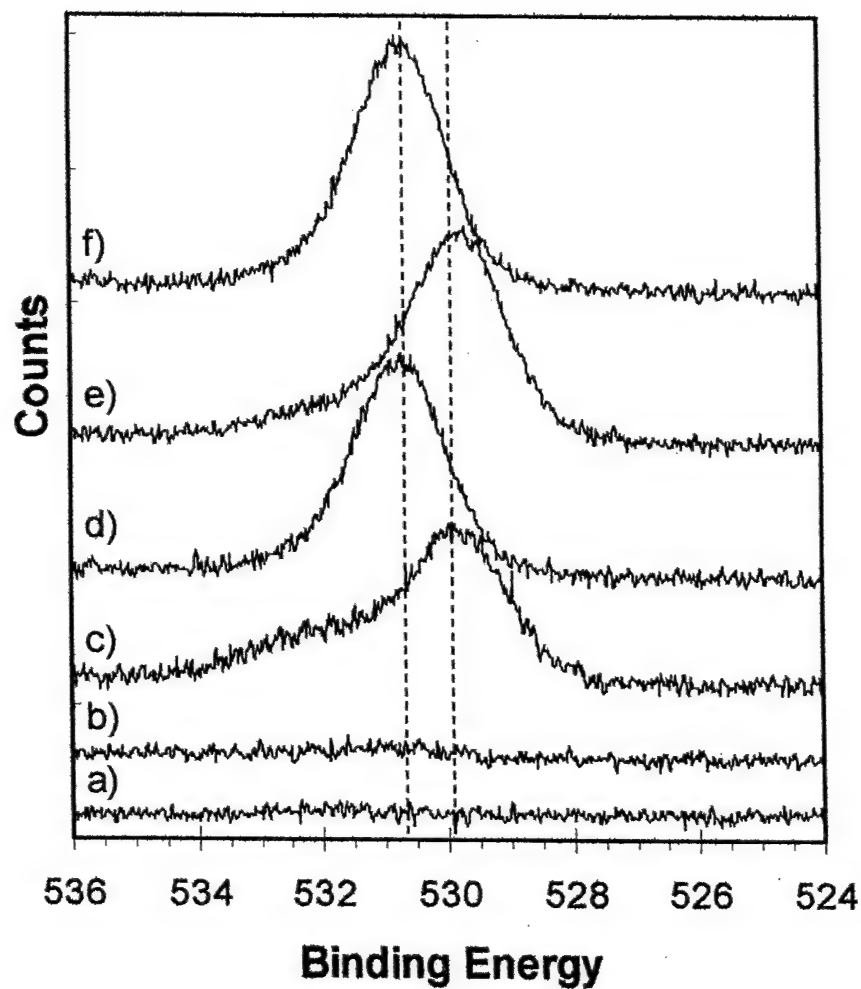


Figure 2. Oxygen 1s XPS spectra for: a) CVC Clean n-GaN, b) 4 Å Hf deposition, c) 4 Å Hf and O₂ plasma, d) 8 Å Hf, O₂ plasma, and 650°C anneal, e) 12 Å Hf and O₂ plasma, f) 650°C final anneal. The peak positions of the initial surface, as well as the final surface are indicated with dashed lines.

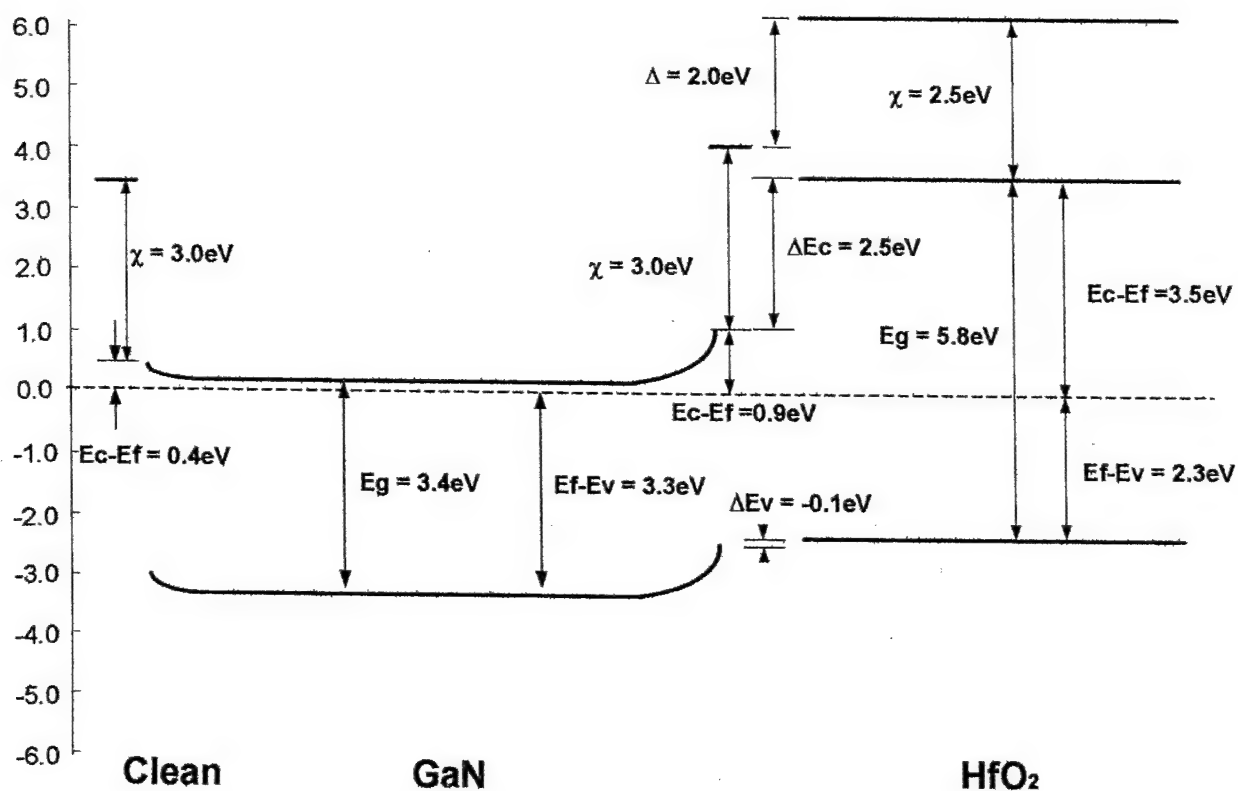


Figure 3. Deduced bands for the clean n-type GaN surface (left) and the interface between n-type GaN and HfO₂ before annealing. The valence band offset, ΔE_v , conduction band offset, ΔE_c , band bending, and interface dipole, Δ , are represented.

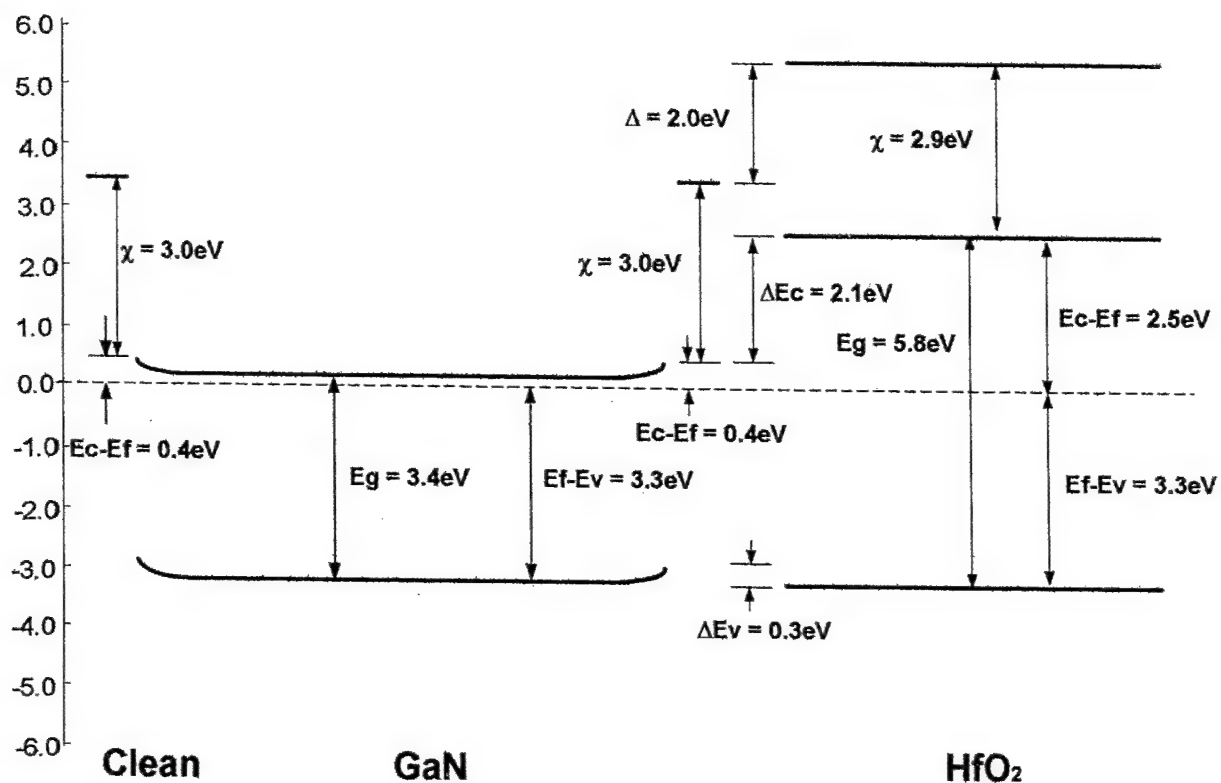


FIGURE 4. DEDUCED BANDS FOR THE CLEAN N-TYPE GAN SURFACE (LEFT) AND THE INTERFACE BETWEEN N-TYPE GAN AND HFO₂ AFTER ANNEALING AT 650 °C. THE VALENCE BAND OFFSET, ΔE_V , CONDUCTION BAND OFFSET, ΔE_C , BAND BENDING, AND INTERFACE DIPOLE, Δ , ARE REPRESENTED.

DEVICE-QUALITY GAN-DIELECTRIC INTERFACES BY 300 °C REMOTE PLASMA PROCESSING

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In previous studies, device quality Si-SiO₂ interfaces and dielectric bulk films (SiO₂) were prepared using a two-step process; i) remote plasma-assisted oxidation (RPAO) to form a superficially interfacial oxide (~0.6 nm) and ii) remote plasma enhanced chemical vapor deposition (RPECVD) to deposit the oxide film. The same approach has been applied to GaN-SiO₂ system. Low-temperature (300°C) remote N₂/He plasma cleaning of the GaN surface, and the kinetics of GaN oxidation using RPAO process and subcutaneous oxidation during the SiO₂ deposition using an RPECVD process have been investigated from analysis of on-line Auger electron spectroscopy (AES) features associated N and O. Compared to single step SiO₂ deposition, significantly reduced defect state densities are obtained at the GaN-dielectric interfaces by independent control of GaN-GaO_x ($x \sim 1.5$) interface formation by RPAO, and SiO₂ deposition by RPECVD.

Key words; GaN-dielectric interfaces, surface leaning, subcutaneous oxidation, Ga₂O₃, SiO₂, MOSd devices

I. INTRODUCTION

GaN has emerged as important material for opto-electronic and high temperature/high power/high frequency device applications. As such, GaN-dielectric insulators for gate dielectrics [1] and surface passivation layers [2], as well as surface cleaning [3,4] have become important issues in device processing. When dielectric layers are formed on a GaN surface by deposition rather than oxidation, the pre-deposition cleaning of the GaN surface is a critical requirement because the initially prepared surface forms the buried device interface. The *in-situ* deposition of the epitaxially grown films, including lattice-matched heterojunctions with other group III-nitride materials, have identified the potential importance for GaN-based metal-insulator-semiconductor (MIS) technology. Deposited amorphous SiO_2 and Al_2O_3 have been the two most promising insulators for III-V semiconductor, mainly because of their wide band gaps. Si_3N_4 is another choice when substrate oxidation during dielectric deposition must be avoided.

When SiO_2 thin films are deposited directly onto Si, Ge, GaAs and CdTe using remote plasma enhanced chemical vapor deposition (RPECVD), these substrates were oxidized superficially by plasma-activated species during the initial stages of film deposition. [5]. These parasitic reactions, or *subcutaneous oxidation processes*, during thin film deposition degrade the electrical characteristics of the interfaces. To prevent subcutaneous oxidation of GaAs and Ge, a thin sacrificial Si layer was deposited before the deposition of SiO_2 thin film [5]. Improved surface passivation of GaAs was obtained by removal of As_2O_3 and subsequent formation of a Ga_2O_3 film [6]. To prepare a device quality Si- SiO_2 interface and dielectric bulk film (SiO_2), a superficially thin Si oxide layer (~ 0.6 nm) was formed on silicon substrate by a remote plasma-assisted oxidation (RPAO) process, and the remainder of the oxide layer is deposited by the

RPECVD process [7,8]. The same RPAO-RPECVD process has been applied to SiC-SiO₂ [9] and GaN-SiO₂ [10], respectively.

In this work, a low-temperature plasma-assisted N ion cleaning process, the kinetics of GaN oxidation and occurrence of subcutaneous oxidation of GaN during plasma enhanced deposition of SiO₂ films have been studied using Auger electron spectroscopy (AES) measurements. Additionally, we report on the effect of subcutaneous oxidation the on degradation of electrical characteristics of GaN metal-oxide-semiconductor (MOS) capacitors.

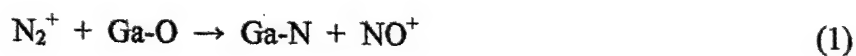
II. EXPERIMENTAL

An epitaxial GaN (0001) layer was directly grown on the *c*-plane of sapphire by hydride vapor phase epitaxy (HVPE) using commercial TDI wafers. Silicon was used as *n*-type dopant, and the thickness of the GaN epitaxial layer was 5 μm . These GaN layers had a electron concentrations of $5\text{-}10 \times 10^{17} \text{ cm}^{-3}$. The 2-inch GaN/sapphire wafers were degreased in acetone, and then methanol, each for 20 minutes. A standard RCA clean was followed by etching in 1:5 NH₄OH:H₂O solutions at 60-80 °C (or in HCl based solutions). Following this, GaN samples were loaded into a multi-chamber system [7-10], which provided chambers for remote plasma-assisted processing and on-line AES measurements. The GaN sample was first exposed to reactive species from a remote N₂/He discharge at 0.02-0.3 Torr. The *in situ* cleaned GaN surface was then oxidized by an RPAO process using a He/O₂ source gas mixture [11]. For the SiO₂ deposition, the flow rates for plasma excited O₂ and He, and down-stream injected 2%-SiH₄ in He were respectively 60, 200 and 10 sccm. The process pressure, substrate temperature and plasma power for both the oxidation and SiO₂ deposition were 0.3 Torr, 300 °C and 30 W at 13.56 MHz, respectively. The experimental procedure was to alternate AES measurements using a 3 keV electron beam with the SiO₂ depositions of 20 s. Post oxide deposition annealing (POA) was carried out at 900 °C for 30 min in an N₂ atmosphere. For the fabrication of GaN MOS

capacitors, a 300 nm Al layer was evaporated after the formation of the gate dielectrics. After an electrode area was defined by a conventional lithography process, post metallization annealing (PMA) was performed at 400 °C for 30 min in forming gas (N_2/H_2).

III. RESULTS AND DISCUSSION

Figure 1 shows differential AES spectra of (i) as-loaded GaN surface (after etching in 1:5 $NH_4OH:H_2O$ solutions), and N_2/He plasma treated GaN surface at 300 °C for 15 min at (ii) 0.02, (iii) 0.1 and (iv) 0.3 Torr, respectively. The N_2/He plasma treatment in the pressure range from 0.02-0.3 Torr reduced residual C below AES detection. Reducing the process pressure of N_2/He plasma from 0.3 to 0.02 Torr, the AES peak ratio of O *KLL* and N *KLL* (O/N) was reduced to a limiting value of ~ 0.06 , which is approximately the same as that of a GaN surface obtained by annealing in NH_3 at 860 °C [4]. By reducing the process pressure from 0.3 to 0.02 Torr during the N_2/He clean, the O coverage on GaN surface (Θ_{ox}) obtained using integrated Auger intensity area ratio of each element [3], decreased from ~ 0.5 to ~ 0.1 monolayer (ML). Wet chemical treatment using 1:1 $HCl:H_2O$ and 3:1 $HCl:HNO_3$ solutions were also used before N_2/He plasma treatment. As shown in Fig. 2, each wet chemical treatment showed differences in the amounts of residual impurities, but the *in situ* N_2/He plasma treatment at 0.02 Torr reduced C and Cl below AES detection as well as the AES O/N ratio to ~ 0.06 . Decreasing the pressure of remote N_2/He plasma process from 0.3 to 0.1 Torr, the active nitrogen species change from neutral N atoms to N^{2+} ions [8, 12]. The enhanced O dissociation of GaN surface at 0.02 Torr can be attributed to the increase of charged particles such as the N_2^+ ion. It is proposed here that the N_2^+ ion reacts with O bonded to Ga atoms on the GaN surface in the following atom exchange reaction, which is favored by the increased bond energy of NO^+ with respect to N_2^+ ,



Following the low-temperature N_2/He plasma-assisted cleaning at 0.02 Torr, the interface and dielectric layer are formed by a two-step process, or RPAO-RPECVD process. The first step is plasma-assisted oxidation process using He/O_2 source gas mixture that forms an ultra-thin Ga_2O_3 layer on the GaN surface. The kinetics of GaN oxidation were determined from analysis of on-line AES features associated with N and O [8,11]. Figure 3 shows log-log plots of the oxide thickness (t_{ox}) versus oxidation time (t) for the RPAO process at 250 and 300 °C, respectively. This process is self-limiting with power law kinetics similar to those for the plasma-assisted oxidation of Si and SiC [8,9]. The oxide thickness versus oxidation time relation is fitted by a power law function of the form, $t_{ox} = \tau_0 t^\beta$, where τ_0 and β are fitting parameters; $t_{ox} = 1.21 t^{0.22}$ (300 °C) and $t_{ox} = 0.74 t^{0.22}$ (250 °C), respectively. The exponential constant, ' β ' of the GaN oxidation at 250-300 °C (~ 0.22) is smaller than the corresponding exponential constants for Si (~ 0.28) [8] and SiC (~ 0.40) [9].

To demonstrate the occurrence of subcutaneous oxidation of GaN during deposition of SiO_2 using the RPECVD process, two different process sequences, shown in Fig. 4, were compared: (i) a direct deposition of SiO_2 on GaN using RPECVD and (ii) two-step process, i.e., RPAO process to form a superficially thin oxide layer (~ 1.0 nm) and deposition of SiO_2 on GaN using RPECVD process. Figure 5 shows a comparison of oxide thickness as a function of SiO_2 deposition time. The oxide thickness of GaN samples was also obtained from analysis of on-line AES features associated with N and O [8,11]. Increasing the SiO_2 deposition time, the difference of oxide thickness between two samples was gradually reduced from the initial value of ~ 1 nm to ~ 0.3 nm. This reduction indicates that ~ 0.7 nm of GaO_x was formed during the direct SiO_2 deposition on GaN sample without RPAO due to the subcutaneous oxidation process. The GaN

samples with RPAO showed nearly linear SiO₂ deposition rate. This means that negligible subcutaneous oxidation occurred, and ~1.0 nm of GaO_x using RPAO process can inhibit the subcutaneous oxidation of GaN during the SiO₂ deposition by RPECVD.

Figure 6 shows the frequency dependence (1 kHz to 1 MHz) of the capacitance-voltage (C-V) characteristics of GaN MOS capacitors using SiO₂ thin films (~30 nm) (i) without RPAO and (ii) with RPAO (or ~1 nm GaO_x), respectively. The gate voltage was swept from accumulation (positive voltage) to depletion (negative voltage) at room temperature in the dark. Compared to the MOS sample without RPAO, the sample with RPAO showed small flat band voltage shift (ΔV_{FB}) at 1 MHz and weak frequency dependence of the capacitance. The characteristics of GaN MOS capacitors (i) without RPAO and (ii) with RPAO were compared as listed in Table I. In the evaluation of expressions for theoretical C-V curves [13], the same fundamental constants in previous report [14] were used. The interface state densities (D_{it}) of both samples were calculated from Terman's method [13].

The minimum values of D_{it} were $3 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ for with RPAO samples and $2 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ for without RPAO samples, respectively. These C-V characteristics indicate that fixed oxide charge and the density of interface trappings states can be reduced by the two-step remote plasma-assisted oxidation-deposition process.

IV. Summary

An N₂/He plasma treatment at low temperature (300 °C) removes residual C and Cl on GaN surface below AES detection, and reduces the AES peak ratio of O *KLL* and N *KLL* (O/N) to ~0.06 (or, ~0.1 monolayer of oxygen coverage of GaN surface). The kinetics of GaN oxidation were determined from analysis of on-line AES features associated with Ga, N and O, and can be fit by an empirical power-law function. An on-line AES study indicates that ~0.7 nm

of GaO_x was formed during the direct SiO_2 deposition on GaN sample due to a subcutaneous oxidation process. Using a two-step process that provides separate and independent control of the interface, an ultra-thin Ga_2O_3 interfacial oxide, and the SiO_2 dielectric, a low interface state density of GaN MOS system was achieved.

ACKNOWLEDGEMENTS

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Figures and Table captions

Figure 1 Differential AES spectra of (i) as-loaded (after etching in 1:5 $\text{NH}_4\text{OH}:\text{H}_2\text{O}$), and N_2/He plasma treated GaN surface at 300 °C for 15 min at (ii) 0.02, (iii) 0.1 and (iv) 0.3 Torr, respectively.

Figure 2 Differential AES spectra of GaN surface after etching in (a) 1:1 $\text{HCl}:\text{H}_2\text{O}$ (RT), (b) 1:1 $\text{HCl}:\text{H}_2\text{O}$ (90 °C) and (c) 3:1 $\text{HCl}:\text{HNO}_3$ (90 °C). After *in situ* N_2/He plasma treatment at 0.02 Torr, C and Cl were reduced below AES measurement limit and O *KLL*/N *KLL* reduce to ~0.06 regardless of varied wet chemical treatments.

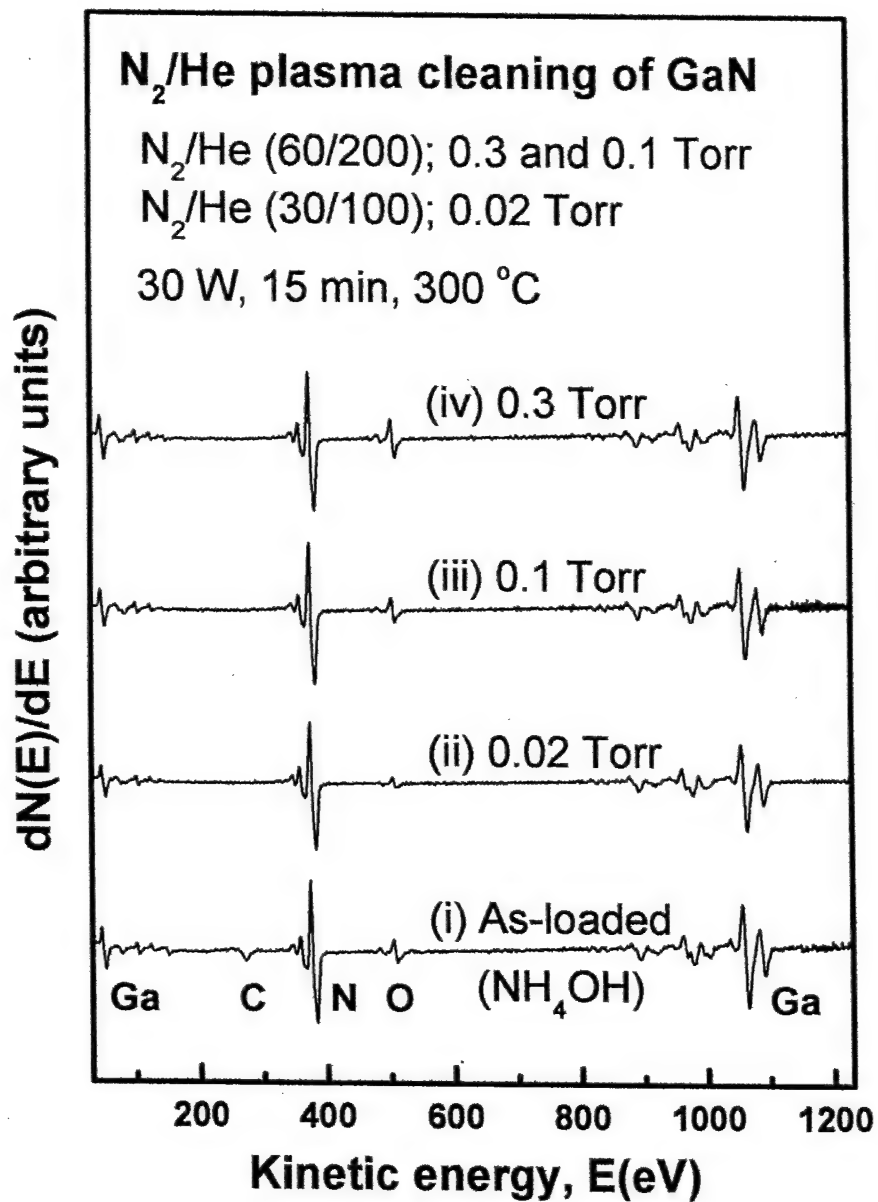
Figure 3 Log-log plots of the oxide thickness (t_{ox}) as a function of oxidation time (t) for the RPAO process using O_2 source gas at 250 and 300 °C, respectively. The straight lines connecting the data points represent a power-law dependence, i.e., $t_{\text{ox}} = \tau_0 t^\beta$, where τ_0 and β are fitting parameters.

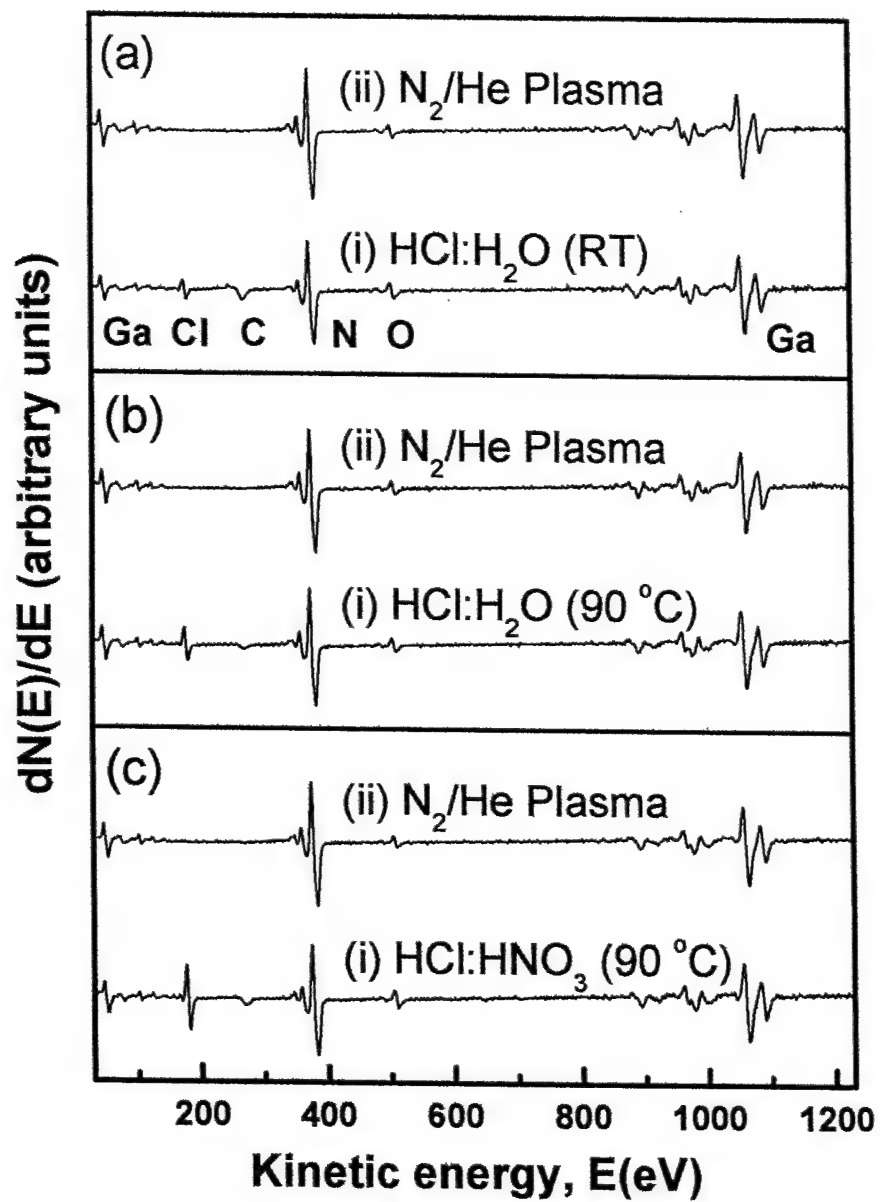
Figure 4 Two different process sequences were used to demonstrate the presence of subcutaneous oxidation of GaN during deposition of SiO_2 . (a) a direct deposition of SiO_2 on GaN using RPECVD process and (b) two-step process, i.e., RPAO process to form a superficially thin oxide layer (~1.0 nm) and deposition of SiO_2 on GaN using RPECVD process.

Figure 5 Comparison of determined oxide thickness of GaN sample (i) without RPAO and (ii) with RPAO as a function of SiO_2 deposition time.

Figure 6 The frequency dependence (1 kHz to 1 MHz) of the C-V characteristics of GaN MOS capacitors (i) without RPAO and (ii) with RPAO.

Table I The characteristics of GaN MOS capacitors (i) without RPAO and (ii) with RPAO. N_f is the oxide fixed charge obtained from the flat band voltage shift (ΔV_{FB}), and D_{it} is the density of interface state densities obtained from the Terman's method.

*Figure 1*

*Figure 2*

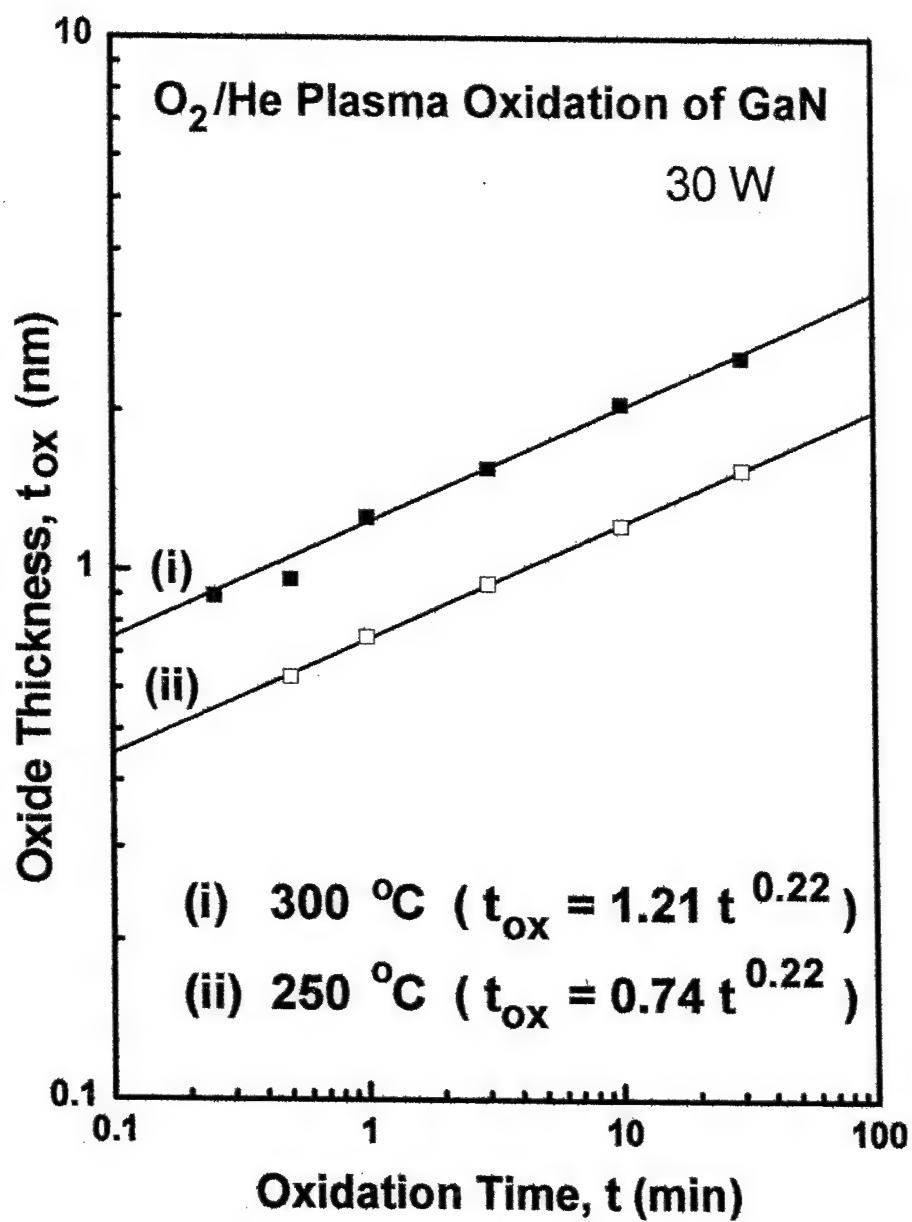


Figure 3

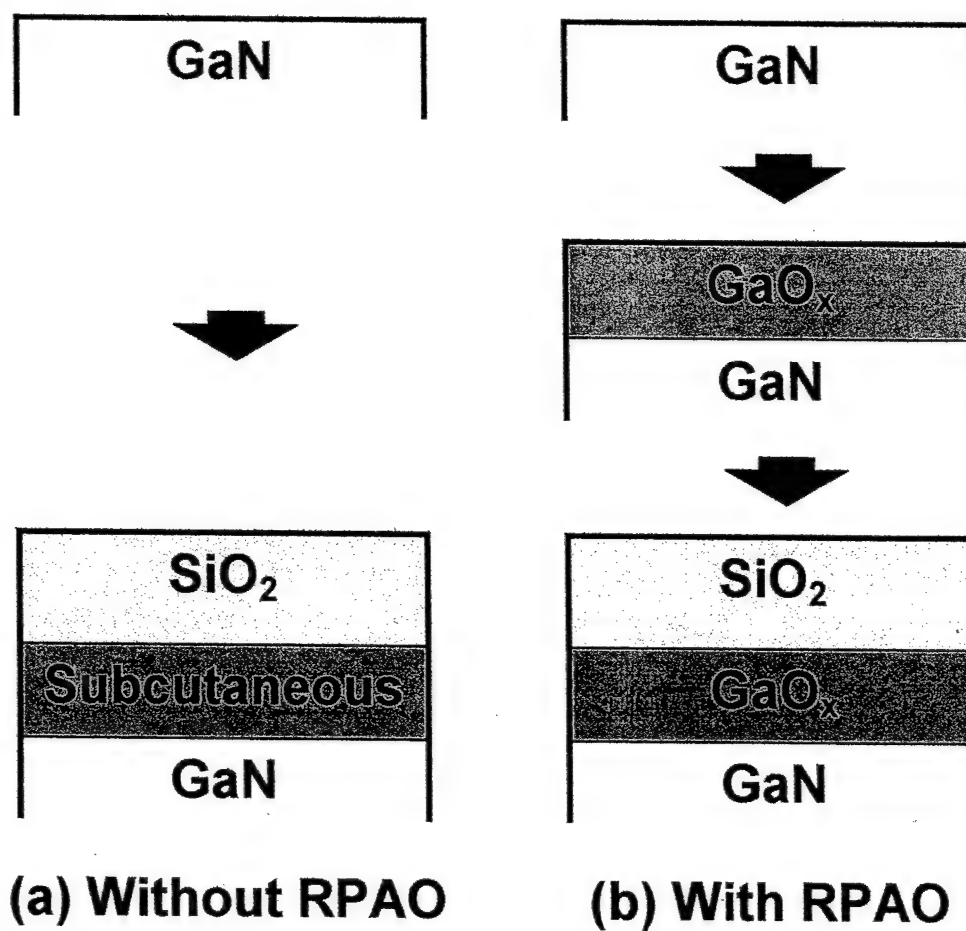


Figure 4

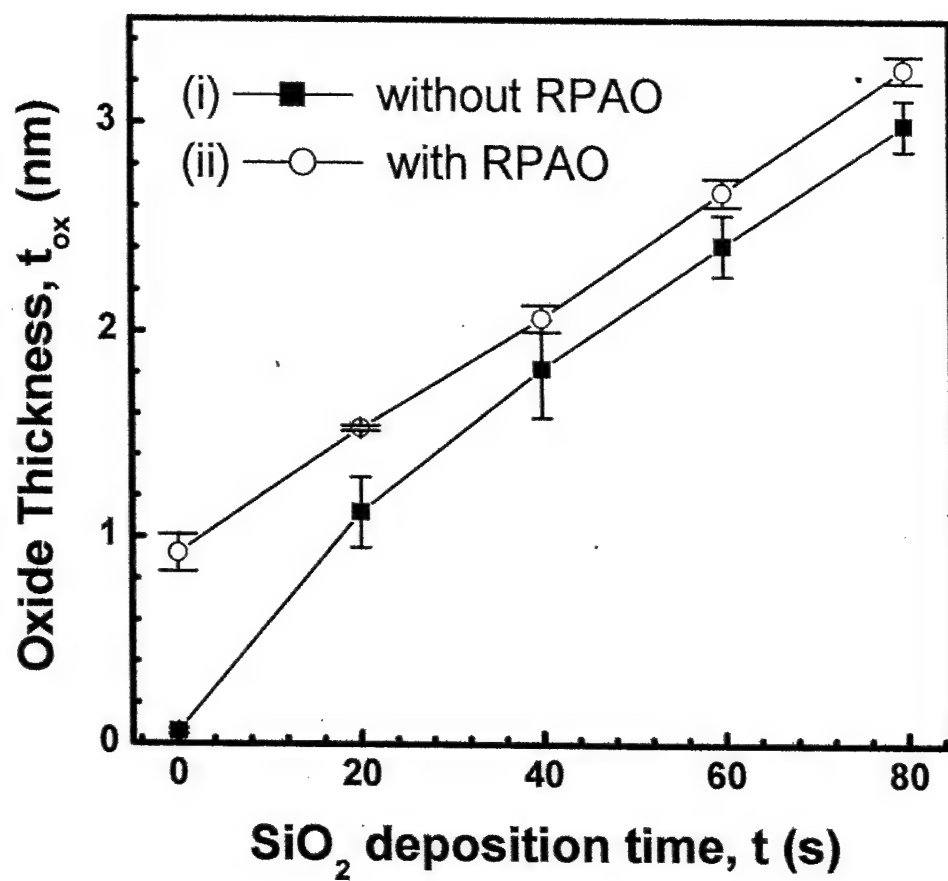


Figure 5

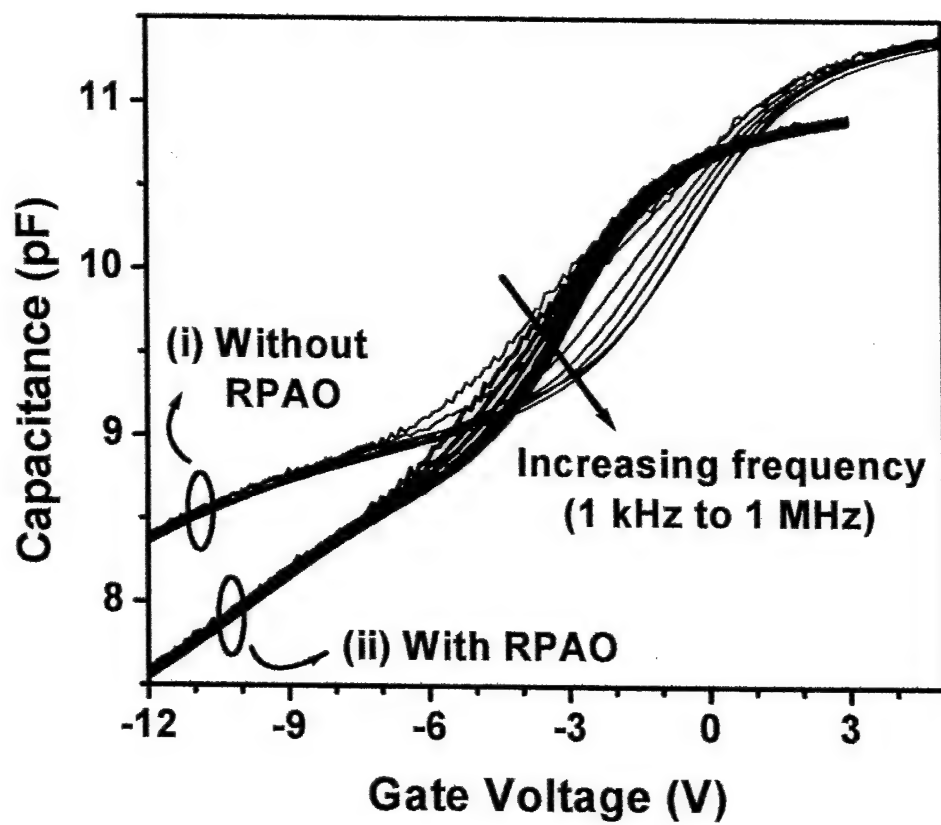


Figure 6

	t_{ox}	ΔV_{FB}	N_{f}	D_{it}
(i) without RPAO	31.2 nm	2.0 V	(-) $1.4 \times 10^{12} \text{ cm}^{-2}$	$2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$
(ii) with RPAO	29.9 nm	-0.5 V	(+) $3.5 \times 10^{11} \text{ cm}^{-2}$	$3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$

Table I

Low-Temperature Preparation of GaN-SiO₂ Interfaces with Low Defect Density (I); Two-Step Remote Plasma-Assisted Oxidation-Deposition Process

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In previous studies, device quality Si-SiO₂ interfaces and dielectric bulk films (SiO₂) were prepared using a two-step process; i) remote plasma-assisted oxidation (RPAO) to form a superficially interfacial oxide (~0.6 nm) and ii) remote plasma enhanced chemical vapor deposition (RPECVD) to deposit the oxide film. The same approach has been applied to GaN-SiO₂ system. Without an RPAO step, subcutaneous oxidation of GaN takes place RPECVD deposition of SiO₂, and on-line Auger electron spectroscopy (AES) indicate a ~0.7 nm subcutaneous oxide. The quality of interface and dielectric layer with/without RPAO process has been investigated by fabricated GaN metal-oxide-semiconductor (MOS) capacitors. Compared to single step SiO₂ deposition, significantly reduced defect state densities are obtained at the GaN-SiO₂ interface by independent control of GaN-GaO_x interface formation by RPAO and SiO₂ deposition by RPECVD.

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I. INTRODUCTION

GaN has emerged as an important material for opto-electronic and high temperature/high power/high frequency device applications. As such, GaN-dielectric insulators for gate dielectrics [1] and surface passivation layers [2] have become important issues in device processing. Researches of GaN metal-insulator-semiconductor (MIS) systems have been focused on reducing fixed oxide charge and interface-trapped charge. For *n*-type GaN MIS systems, interface state density (D_{it}) in the range of low-to-mid $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ has been obtained without *in-situ* native oxide removal and thin intermediate layer (or sacrificial layer) preparation [1]. These results are remarkably different from the other compound semiconductors where surface passivation has been important issue to avoid thin native oxide formation between deposited oxide and substrate. Considering the deep depletion without severe Fermi-level pinning, and the low D_{it} of *n*-type GaN MIS systems, the native oxide of GaN is exempt from the critically undesirable factors such as multiple type oxides, thermodynamic instability, metallic residue, and smaller bandgap than that of the semiconductor. In the cases of GaAs metal-oxide-semiconductor (MOS) systems, improved surface passivation was initially obtained by removal of As_2O_3 and subsequent formation of a few monolayers of Ga_2O_3 film or $(\text{Ga}_2\text{O}_3)_{1-x}(\text{Gd}_2\text{O}_3)_x$ [3-5].

The main difference of GaN from other III-V semiconductors, such as GaAs and GaP, is the volatility of N oxide species, e.g., NO, N_2O , etc. This suggests that thin native oxide of GaN can be used to control semiconductor-deposited dielectrics interface. The purpose of present work is to investigate that a controlled superficially thin native oxide of GaN can improve the quality of interface and dielectric layer of GaN MOS system. For the oxide film deposition by plasma-assisted process, *ex situ* wet chemical and *in situ* removal of the air-grown native oxide does not guarantee that there is no interfacial oxide because the presence of oxidant and excitation very often leads to the growth of an oxide on the substrate surface. When SiO_2 thin

films were deposited on Si, Ge, GaAs and CdTe using remote plasma enhanced chemical vapor deposition (RPECVD), the substrates were slightly consumed by plasma-activated species that diffused through the deposited oxide layer and oxidized the underlying substrate [6-8]. These parasitic reactions, or subcutaneous oxidation, during oxide film deposition by RPECVD process degrade the electrical characteristics of the interface. To prevent the subcutaneous oxidation of the GaAs and Ge, a thin sacrificial Si layer was deposited before the deposition of SiO₂ thin film [6-8]. To prepare device quality Si-SiO₂ interface and dielectric bulk film (SiO₂), the superficially thin oxide layer (~0.6 nm) is formed on silicon substrate by a remote plasma-assisted oxidation (RPAO) process, and the remainder of the oxide layer is deposited by a RPECVD process [9]. After formation of ~0.6 nm of oxide in ~15 s, the oxidation rate slows down to ~0.3-0.4 nm/min. Therefore, during plasma-enhanced deposition at rates of ~2.5-5 nm/min, plasma-activated O species are consumed faster by deposition reactions with SiH₄ than by continued oxidation at the buried Si-SiO₂ interface [10]. The same RPAO-RPECVD process has been applied to SiC [11], Ge [12], and GaN [13] and has yielded semiconductor-dielectric interface with reduced net oxide charges compared with the direct deposition of SiO₂ film on semiconductor substrate.

On the other hand, low D_{it} of GaN MIS systems also attributed to the possible underestimation of actual D_{it} . In a wide band gap semiconductor, the Terman method at room temperature can lead to gross underestimation of D_{it} because interface states more than ~0.6 eV above the valence (or below the conduction) band edge cannot follow changes in dc bias at room temperature [14]. Therefore, high temperature or photo-assisted $C-V$ measurements have been suggested to estimate D_{it} over a significant portion of the wide band gap. The present work suggests another introduced error in the estimation of D_{it} using Terman method due to the wide

band gap of GaN. Terman method relies on a high-frequency C - V measurement at a sufficiently high frequency that interface traps are assumed not to respond, but they respond to the slowly varying dc gate voltage and cause the C - V curve "stretch out" along the gate voltage axis as interface trap occupancy changes with gate bias [15, 16]. In the estimation of D_{it} using Terman method, it is well known that doping concentration should be known exactly in order to compare the difference between the measured and calculated C - V curves. However, doping concentration for calculated C - V curves have been selected until a close fit of C - V curves was obtained over the entire voltage range because the C - V characteristics of GaN MOS capacitors showed deep depletion instead of inversion. Then, the C - V curve "stretch out" associated with uniformly distributed D_{it} could be misinterpreted as an increased doping concentration, and lead to the underestimation of D_{it} . High-low frequency method or conductance method, which does not require theoretical curve to compare with measured curve, can be considered to reduce the uncertainty associated with doping concentration in C - V characterizations of GaN MOS system. However, due to high series resistance (R_s) and system noise, quasistatic or low (below 100 Hz) frequency C - V curve has not been reported, and conductance method has been limitedly used for GaN MOS analysis. In addition, there are side contact effects on the capacitance properties [17] for the MOS system using thin epitaxial layers grown on insulating substrate. For the GaN MOS structures, it is also difficult to properly extract oxide fixed charge from flat band voltage shift (ΔV_{fb}). The extraction of fixed charge from ΔV_{fb} have several uncertainty such as (i) compensated effect [14] among several types of charge, (ii) uncertain doping concentration of GaN MOS system which was usually obtained from close fit of C - V curve, and (iii) assumption of both the electron affinity of GaN and the work function of the Al gate as 4.1 eV.

In this work, the occurrence of subcutaneous oxidation of GaN during plasma-enhanced deposition of SiO₂ films has been studied using Auger electron spectroscopy (AES) measurements. The quality of interface and dielectric layer with/without RPAO process was investigated by fabricated GaN MOS capacitors.

II. EXPERIMENTAL

The epitaxial GaN (0001) layer was directly grown on the *c*-plane of sapphire by hydride vapor phase epitaxy (HVPE) from TDI. Silicon was used as *n*-type dopant, and the thickness of the GaN epitaxial layer was 5 μm. The as grown GaN layer had an electron concentration of $5 \cdot 10 \times 10^{17} \text{ cm}^{-3}$. As-received 2-inch GaN epi-wafer on sapphire was degreased in organic solvents (acetone, methanol) each for 20 min. After wet chemical treatments using 1:1:5 NH₄OH:H₂O₂:H₂O solutions at ~80 °C and followed etching in 1:5 NH₄OH:H₂O solutions at ~80 °C, GaN samples were loaded into a multi-chamber system [10], which provided a separate remote plasma-assisted process and on-line AES measurement.

To investigate the initial stages of oxidation of the GaN surface, the AES measurements using 3 keV electron beam was performed following each process step. As-loaded GaN sample was exposed to reactive species from a remote N₂/He discharge at 0.02 Torr in order to reduce residual contaminants after wet chemical treatments [18]. Superficially thin GaO_x (~1 nm), with a composition close to Ga₂O₃ or $x \sim 1.5$, was formed by the RPAO process at 0.3 Torr using O₂ source [18], and a thin SiO₂ film was deposited by RPECVD process at 0.3 Torr [10]. The substrate temperature was 300 °C, and plasma power was 30 W at 13.56 MHz. The experimental procedure was to alternate AES measurements with the SiO₂ deposition for 20 s, i.e., interrupted processing and AES analysis cycles.

For the fabrication of GaN MOS capacitors, SiO₂ films were deposited onto wet chemical treated GaN samples with/without RPAO. After gate dielectric insulator deposition, the sample was rapid-thermal annealed at ~900 °C for 30 s in Ar atmosphere. A 300 nm Al layer was evaporated and defined by the conventional lithography process. For GaN MOS capacitors without RPAO, post metallization annealing (PMA) was performed at 400 °C for 30 min in forming gas (N₂/H₂). The electrical properties of GaN MOS capacitors were investigated using HP 4284A (precision LCR meter). The area of device under a test was 4 × 10⁻⁴ cm².

III. RESULTS AND DISCUSSION

A. Subcutaneous oxidation of GaN during deposition of SiO₂

To demonstrate subcutaneous oxidation of GaN during deposition of SiO₂, two different process sequences, shown in Fig. 1, were used: (a) a direct deposition of SiO₂ on GaN using RPECVD process and (b) two-step process, i.e., RPAO process to form a superficially thin RPAO oxide layer (~1.0 nm), or GaO_x with x ~ 1.5 [18], and deposition of SiO₂ on GaN using RPECVD process. Figure 2 displays differential AES spectra for (i) the *in situ* N₂/He plasma cleaned GaN sample followed by (ii) - (vi) the SiO₂ deposition on GaN sample for 20-160 s. After the N₂/He plasma treatment of GaN surface, residual C and Cl were reduced below AES detection, and AES peak ratio of O *KLL* and N *KLL* was ~0.06 (~0.1 monolayer of oxygen coverage on GaN surface) [18]. Increasing the deposition time of SiO₂ film, the N *KLL* (~378 eV) and Ga *LMM* (~1061 eV) features mainly associated with Ga-N bonding in the GaN substrate decreased in strength while O *KLL* (~506 eV) feature mainly associated with O-Si bonding in the deposited oxide layer increased. Figure 3 displays differential AES spectra for (i) the RPAO process of GaN sample using O₂ source gas followed by (ii) - (vi) the SiO₂ deposition

on GaN sample for 20-160 s. Note that N *KLL* features of both samples in Fig. 2 and 3 disappeared at nearly the same SiO₂ deposition time, 120 s. In addition, the Ga *LMM* features of both samples show similar intensity after the deposition of SiO₂ for 160 s. This indicates that oxide thickness (t_{ox}) of both samples became similar after the deposition of SiO₂ film for 120 s.

Figure 4 shows a comparison of determined t_{ox} of GaN samples shown in Fig. 2 and 3 as a function of SiO₂ deposition time. Assuming the negligible dependence of electron escape depth on oxide overlayer, i.e., GaO_x or SiO₂, oxide thickness (t_{ox}) is obtained from [18 and reference therein]

$$t_{ox} = \lambda \ln \left(1 + \frac{I_N^o}{I_O^o} \times \frac{I_O}{I_N} \right) \quad (1)$$

where, I_N = N *KLL* Auger electron intensity from the GaN substrate,
 I_N^o = N *KLL* Auger electron intensity from the clean GaN substrate,
 I_O = O *KLL* Auger electron intensity from the thin GaO_x layer,
 I_O^o = O *KLL* Auger electron intensity from the thick GaO_x layer,
 λ = electron escape depth for O and N, ~1 nm.

The difference of t_{ox} between two samples was gradually reduced by increasing SiO₂ deposition time from the initial value of ~1 nm, and saturated to ~0.3 nm. This reduction indicates that ~0.7 nm of GaO_x was formed during the direct SiO₂ deposition on GaN sample without RPAO due to the subcutaneous oxidation process. The nearly linear SiO₂ deposition rate of the sample with RPAO means that there occurred negligible subcutaneous oxidation, and ~1.0 nm of GaO_x using

RPAO process (or several monolayer of a sacrificial Si) can inhibit the subcutaneous oxidation process of GaN during the SiO₂ deposition.

Figure 5 displays the peak shift of non-differentiated AES spectra by the SiO₂ deposition for (ii) 20, (iii) 40, (iv) 60, (v) 80 and (vi) 180 s on GaN samples (a) without RPAO and (b) with RPAO. Non-differentiated AES spectrum of thick GaO_x sample, obtained by remote O₂/He plasma oxidation of GaN sample for 30 min, is included as a reference in Fig. 5 (b). AES O *KLL* feature at ~505.5 eV of the GaN sample with RPAO, shown in Fig. 5(b), gradually shifts to lower energy as the SiO₂ deposition time increased. This gradual peak shift (~4 eV) of O *KLL* feature indicates that O-Ga bonds change to O-Si bonds. For the direct deposition of SiO₂ on cleaned GaN sample without RPAO, shown in Fig. 5(a), O *KLL* feature after the deposition of SiO₂ for 20 s was located ~1.5 eV higher position than that of thick SiO₂ films (> 3 nm) and gradually shifted to lower energy as the SiO₂ deposition time increased. This peak shift demonstrates that thin GaO_x, or subcutaneous oxide, was formed during the direct SiO₂ deposition on GaN sample.

B. GaN MOS system with/without RPAO

The quality of interface and dielectric layer (i) without and (ii) with RPAO process was compared by the fabricated GaN MOS capacitors. The RPAO process was performed for 30 s to form the RPAO oxide of ~1.0 nm, and the RPECVD process was performed for 12 min to deposit SiO₂ of ~40 nm. Note that both MOS capacitor (i) without RPAO and (ii) with RPAO have interfacial GaO_x layer below SiO₂ film because subcutaneous oxide (~0.7 nm) was formed at the sample without RPAO. In this section, we discuss a significant role of (i) subcutaneous oxide and (ii) RPAO oxide in determining the electrical properties of the semiconductor/oxide interface. Compared to the MOS sample with RPAO, the sample without RPAO showed a large

ΔV_{fb} to the positive voltage direction and frequency dependence in depletion region. Thus, PMA was performed for the sample without RPAO at 400 °C for 30 min in forming gas (N_2/H_2).

Consider first conductance-voltage (G - V) characteristics of GaN MOS capacitors (i) without RPAO before/after PMA and (ii) with RPAO before PMA measured at room temperature and 1 MHz. Figure 6 displays the measured G - V curves that have clear peaks of interface trap loss and negligible oxide loss. The value of R_s determined from measured capacitance and conductance in accumulation was ~ 50 -70 Ω . This relatively low value of R_s for GaN MOS system is attributed to thick (~ 5 μm) GaN epi-layer with high doping concentration (~ 5 - 10×10^{17} cm^{-3}). The low and symmetric base line of G - V curve indicates that there is no significant trapping effects and charge injection into the superficially thin RPAO oxide. For the electron-beam deposited Ga_2O_3 film where the Ga_2O_3 was used as a bulk oxide of MOS system [19,20], interface trap loss is masked by high oxide loss. The conductance peak heights of (i) without RPAO before PMA, (ii) without RPAO after PMA, and (iii) with RPAO before PMA were ~ 2.4 , 1.5 and 0.5 μS , respectively. Since these samples have nearly similar values of R_s and oxide capacitance (C_{ox}), D_{it} of each sample will be approximately proportional to the measured conductance peak heights.

To estimate the distribution of D_{it} using Terman method, C - V curves of each sample were measured at room temperature and 1 MHz. In the evaluation of expressions for theoretical C - V curves [15,16], the same fundamental constants as in a previous report [21] were used. The relative dielectric constant of GaN is taken as 9.5. The intrinsic carrier concentration (n_i) is 2.0×10^{-10} cm^{-3} for GaN at room temperature. Both the electron affinity of GaN and the work function of the Al gate are assumed as 4.1 eV. Figure 7 shows measured and calculated C - V curve of GaN MOS capacitor with RPAO. Also shown is the measured conductance. The calculated C - V curve

was obtained using net donor concentration (N_D) of $1.7 \times 10^{18} \text{ cm}^{-3}$ and fixed oxide charge of $3.5 \times 10^{11} \text{ cm}^{-2}$ (or ΔV_{fb} of -0.6 V). These values were determined from a close fit of measured $C-V$ curve over the entire voltage range. The measured $C-V$ curve shows small deviation from the calculated $C-V$ curve between -1 to -7 V. Note that this deviation cannot be attributed to interface states because the measured curve sharpened rather than stretched. Figure 8 displays the I/C^2-V characteristics. Two linear lines fit the characteristics, and N_D obtained from the slope was increased from the initial value of $1.5 \times 10^{18} \text{ cm}^{-3}$ to $1.7 \times 10^{18} \text{ cm}^{-3}$. It is not clear whether this result is caused by the actual change in N_D or voltage and capacitance changes associated with interface states. Figure 9 shows the distribution of D_{it} by applying Terman method. The minimum D_{it} was estimated as $\sim 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at $\sim 0.45 \text{ eV}$ below conduction band edge. For the sample without RPAO before/after PMA, as shown in Fig. 10, there were severe flatten out in the measured $C-V$ curves. When the measured $C-V$ curves were partially fit above $\sim 30 \text{ pF}$, measured curves agreed with calculated curves. N_D was $2.7 \times 10^{18} \text{ cm}^{-3}$ for the sample before PMA and $2.0 \times 10^{18} \text{ cm}^{-3}$ for the sample after PMA, respectively. These results indicate that the $C-V$ curve "stretch out" along the gate voltage axis, which is associated with interface trap occupancy changes, can be misinterpreted as an increased N_D .

Since high-low frequency method does not require theoretical curve to compare with measured curve, this method can reduce the uncertainty of the extraction of D_{it} associated with doping concentration. In this study, $C-V$ curves measured at 1 MHz and 3 kHz were used as high and low frequency $C-V$ curves, respectively. The actual D_{it} will be higher than estimated value using this method because 3 kHz frequency is not sufficiently low that slow interface traps respond. In addition, the gate voltage where low and high $C-V$ curves showed the maximum capacitance difference (ΔC_{max}) can be used to determine the energy level of minimum D_{it} . The

capacitance difference between low and high frequency is due to the electron emission and capture by interface states. If each energy level has the same values of D_{it} and time constant of electron emission, the capacitance difference will be continuously increased with gate bias sweep from accumulation to depletion. In fact, capacitance difference showed maximum value and gradually decreased to negligible value because the time constant for electron emission from interface states increase exponentially with energy from the conduction band edge. Then, a limiting energy where D_{it} can be investigated without underestimation will be obtained at the gate voltage of ΔC_{max} . Figure 11 shows the frequency dependence (1 kHz to 1 MHz) of the C - V characteristics of GaN MOS capacitors (i) without RPAO after PMA and (ii) with RPAO. The gate voltage was swept from positive to negative voltage at room temperature. Figure 12 shows the distribution of D_{it} as a function of gate voltage calculated from [15,16]

$$D_{it} = \frac{C_{ox}}{q} \left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \quad (2)$$

where, C_{lf} is the capacitance measured at low frequency (or 3 kHz) and C_{hf} is the capacitance measured at high frequency (or 1 MHz). The minimum D_{it} was determined at the gate voltage where low and high C - V curves showed ΔC_{max} . For the C - V curves measured at 1 MHz, shown in Fig. 11, the values of C/C_{ox} at the voltage of ΔC_{max} were ~ 0.88 - 0.89 . This small difference in the values of C/C_{ox} indicates that the minimum D_{it} was determined at the similar energy level. Minimum D_{it} of (i) without and (ii) with RPAO was $\sim 4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at -2.5 V and $\sim 7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at -4.1 V , respectively. Figure 13 shows the distribution of D_{it} over the band gap energy near conduction band edge using Terman method and high-low frequency method. When

the extracted values of D_{it} were compared at ~ 0.3 eV, where ΔC_{\max} was observed, D_{it} using Terman method is ~ 2 times smaller than that using high-low frequency method. Note that calculated curve without D_{it} was obtained using N_D from a close fit of C - V curve, and the actual energy level for minimum D_{it} was located at deeper level than ~ 0.3 eV.

Conductance method was also used to clarify the estimated D_{it} using high-low frequency method. Figure 14 and 15 show the parallel conductance loss (G_p/ω) versus angular frequency (ω) curves at selected gate voltages. Assuming negligible series resistance, G_p/ω was obtained from [16]

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (3)$$

where G_m is the measured conductance and C_m is the measured capacitance. From the graphically determined standard deviation of band bending (σ_s) and universal function (f_D) as a function of σ_s , D_{it} of each sample was calculated from [16]

$$D_{it} = \left(\frac{G_p}{\omega} \right)_{f_p} [q f_D(\sigma_s)]^{-1} \quad (4)$$

where f_p is the frequency corresponding to the peak value G_p/ω . The determined values of f_D were about 0.34-0.38 for the sample without RPAO and 0.24-0.26 for the sample with RPAO, respectively. Figure 16 shows D_{it} from the conductance measurements in Fig. 14 and 15 along with D_{it} from the high-low frequency method in Fig. 12. Both methods well indicate that D_{it} of

(i) without RPAO after PMA is ~5 times larger compared to that of (ii) with RPAO. Therefore, it is clear that the two-step (RPAO-RPECVD) process can effectively reduce D_{it} of the GaN MOS system.

C. High temperature and photo-assisted C - V measurements

In order to estimate D_{it} over a significant portion of the wide band gap, there have been high temperature C - V method [22-24] and photo-assisted C - V method [21,22,25]. The GaN MOS sample with RPAO was investigated using these two methods.

Figure 17 shows the C - V characteristics measured at 25-200 °C in the dark. Also shown is the change in polarization charge (ΔQ) [23] by increasing temperature. As reported by Matocha *et al.* [23], our C - V curves also showed positive shift with increasing temperature. They reported that their large positive shift (~2 V) was caused by the pyroelectric polarization of GaN because the change in the semiconductor bulk potential (E_c-E_f) and interface trap charge (Q_{it}) with increasing temperature make negligible ΔV_{fb} (below 0.1 V) to the negative voltage direction. For the capacitor with RPAO, shown in Fig. 17, calculated ΔV_{fb} from the change in E_c-E_f was about -0.06 V with increasing temperature from 25 to 200 °C. The determined pyroelectric charge coefficient was $\sim 4.9 \times 10^9$ q/cm²-K. As shown in Fig. 17, however, C - V curves were stretched along the voltage axis and flatten out with increasing temperature. This indicates that electron capture/emission associated interface traps were increased at high temperature and not negligible in the measured positive shift of V_{fb} .

Figure 18 shows the photo-assisted C - V characteristics measured at room temperature. The sweep rate of gate bias was 100 mV/s. From N_D of 1.7×10^{18} cm⁻³, the threshold voltage was determined as about -18 V. The bias first swept from accumulation (+3 V) to deep depletion (-21 V) in the dark. While the bias remained at -21 V, the sample was illuminated by ultraviolet lamp

(365 nm) until the measured capacitance saturated. After the capacitance saturated, the lamp was turned off and the bias was swept back to accumulation in the dark. Due to the higher photo-saturated capacitance (~ 31 pF) than the expected inversion capacitance (~ 25 pF), "interface state ledge" [14,26,27] was not observed, and photo-induced hysteresis (ΔV_p) was obtained within the limited voltage range. Tungsten bulb or microscope illumination can make the same value of photo-saturated capacitance with a reduced ΔV_p . The discrepancy between photo-saturated capacitance and the expected inversion capacitance was also reported [21,22], and attributed to the small minority-carrier recombination rate rather than charge transfer from interface states [22]. In this study, the photo-saturated capacitance was quite similar to the saturated capacitance measured at 200 °C as well as that of MOS sample without RPAO.

Details of high temperature C - V and photo-assisted C - V will be discussed in a separate report. It would be interesting to investigate the high temperature C - V characteristics of non-polar (or Ga and N terminated surface) GaN MOS structure, and the photo-assisted C - V characteristics by varying the gate voltage sweep rate.

IV. CONCLUSION

A low temperature RPAO process for interface formation and passivation has been extended from Si and SiC to GaN. The process provides the control of ultra-thin interfacial layers that passivate the GaN substrate, preventing a parasitic or subcutaneous oxidation of the substrate during plasma deposition of SiO_2 . Without RPAO step, subcutaneous oxidation of GaN takes place during RPECVD deposition of SiO_2 , and on-line AES indicate a ~ 0.7 nm subcutaneous oxide. A two-step process (RPAO-RPECVD) has been shown to result in significantly reduced interfacial trapping compared to a single step SiO_2 deposition that does not

include the RPAO step. High-low frequency method and conductance method indicate that D_{it} of GaN MOS sample without RPAO is ~5 times larger than that of the sample with RPAO. Improved GaN-dielectric interface properties will be obtained by changing O_2/He plasma oxidation time to minimize RPAO oxide thickness as a superficially thin (~0.6-1.0 nm) oxide, and following remote plasma-assisted interface nitridation step that introduces approximately one monolayer of nitrogen atoms at the GaN-gallium oxide interface. Also, post oxide deposition anneal and forming gas anneal need to be investigated to obtain optimized processing conditions.

The remote plasma processing can be extended to following applications; (i) the gate dielectric insulator of GaN MOS field effect transistor (MOSFET), (ii) the passivation layer of AlGaIn/GaN high electron mobility transistor (HEMT), and (iii) the intermediating layer prior to the RPAO process of other III-V materials such as GaAs and GaP. For the AlGaIn/GaN HEMT, the RPAO oxide will be mixture of Al_2O_3 and Ga_2O_3 because RPAO process will be performed on AlGaIn. For the GaAs and GaP devices, sacrificial GaN layers are formed prior to the RPAO process since the key of this study is the volatility of N-oxide species, e.g., NO, N_2O , etc. The non-volatility of As and P oxides means RPAO process cannot be applied directly GaAs or GaP.

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Figure captions

Figure 1 Two different process sequences were used to demonstrate the presence of subcutaneous oxidation of GaN during deposition of SiO₂. (a) a direct deposition of SiO₂ on GaN using RPECVD process and (b) two-step process, i.e., RPAO process to form a superficially thin RPAO oxide layer (~1.0 nm), or GaO_x with $x \sim 1.5$ and deposition of SiO₂ on GaN using RPECVD process.

Figure 2 Differential AES spectra for (i) the *in situ* N₂/He plasma cleaned GaN sample followed by (ii) – (vi) the SiO₂ deposition on GaN sample for 20–160 s. Initial oxide thickness (t_{ox}) prior to SiO₂ film deposition on GaN sample was below 0.1 nm.

Figure 3 Differential AES spectra for (i) the RPAO process of GaN sample using O₂ source gas followed by (ii) – (vi) the SiO₂ deposition on GaN sample for 20–160 s. Initial oxide thickness (t_{ox}) prior to SiO₂ film deposition on GaN sample was ~1.0 nm.

Figure 4 Comparison of determined oxide thickness (t_{ox}) of both GaN sample, shown in Fig. 2 and 3, as a function of SiO₂ deposition time (t).

Figure 5 Peak shift of non-differentiated AES spectra by the SiO₂ deposition for (ii) 20, (iii) 40, (iv) 60, (v) 80 and (vi) 180 s on GaN samples (a) without RPAO and (b) with RPAO.

Figure 6 Conductance-voltage (G - V) characteristics of GaN MOS capacitors (i) without RPAO before/after PMA and (ii) with RPAO measured at room temperature and 1 MHz in the dark.

Figure 7 Calculated and measured C - V curve of the GaN capacitor with RPAO at room temperature and 1 MHz. Also shown is the measured conductance.

Figure 8 I/C^2 characteristics as a function of gate voltage. Net doping concentration (N_D) obtained from the slope was $1.5 \times 10^{18} \text{ cm}^{-3}$ and $1.7 \times 10^{18} \text{ cm}^{-3}$.

Figure 9 Distribution of the density of interface state (D_{it}) of GaN MOS capacitor with RPAO using Terman method.

Figure 10 Calculated and measured C - V curve of the GaN capacitors without RPAO before/after PMA at room temperature and 1 MHz.

Figure 11 Frequency dependence (1 kHz to 1 MHz) of the C - V characteristics of GaN MOS capacitors (i) without RPAO after PMA and (ii) with RPAO.

Figure 12 Density of interface state (D_{it}) of GaN MOS capacitors (i) without RPAO and (ii) with RPAO using high-low frequency method. The minimum D_{it} was determined at the gate voltage where low and high C - V curves showed the maximum capacitance difference (ΔC_{max}). Then, minimum D_{it} of (i) without and (ii) with RPAO was $\sim 4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at -2.5 V and $\sim 7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at -4.1 V , respectively.

Figure 13 Distribution of the density of interface state (D_{it}) of GaN MOS capacitor with RPAO using Terman method and high-low frequency method.

Figure 14 Parallel conductance loss (G_p/ω) versus angular frequency (ω) curves measured at 25 °C for GaN MOS capacitor without RPAO after PMA. The graphically determined standard deviation of band bending (σ_s) was 0.5-0.9 (in the unit of kT/q).

Figure 15 Parallel conductance loss (G_p/ω) versus angular frequency (ω) curves measured at 25 °C for GaN MOS capacitor with RPAO. The graphically determined standard deviation of band bending (σ_s) was 1.7-1.9 (in the unit of kT/q).

Figure 16 Density of interface state (D_{it}) of GaN MOS capacitors (i) without RPAO after PMA and (i) with RPAO using conductance method and high-low frequency method.

Figure 17 C - V characteristics of GaN MOS capacitors with RPAO measured at 25-200 °C in the dark. Also shown is the change in polarization charge (ΔQ) by increasing temperature [23].

Figure 18 Photo-assisted C - V characteristics of GaN MOS capacitors measured at room temperature and 1 MHz.

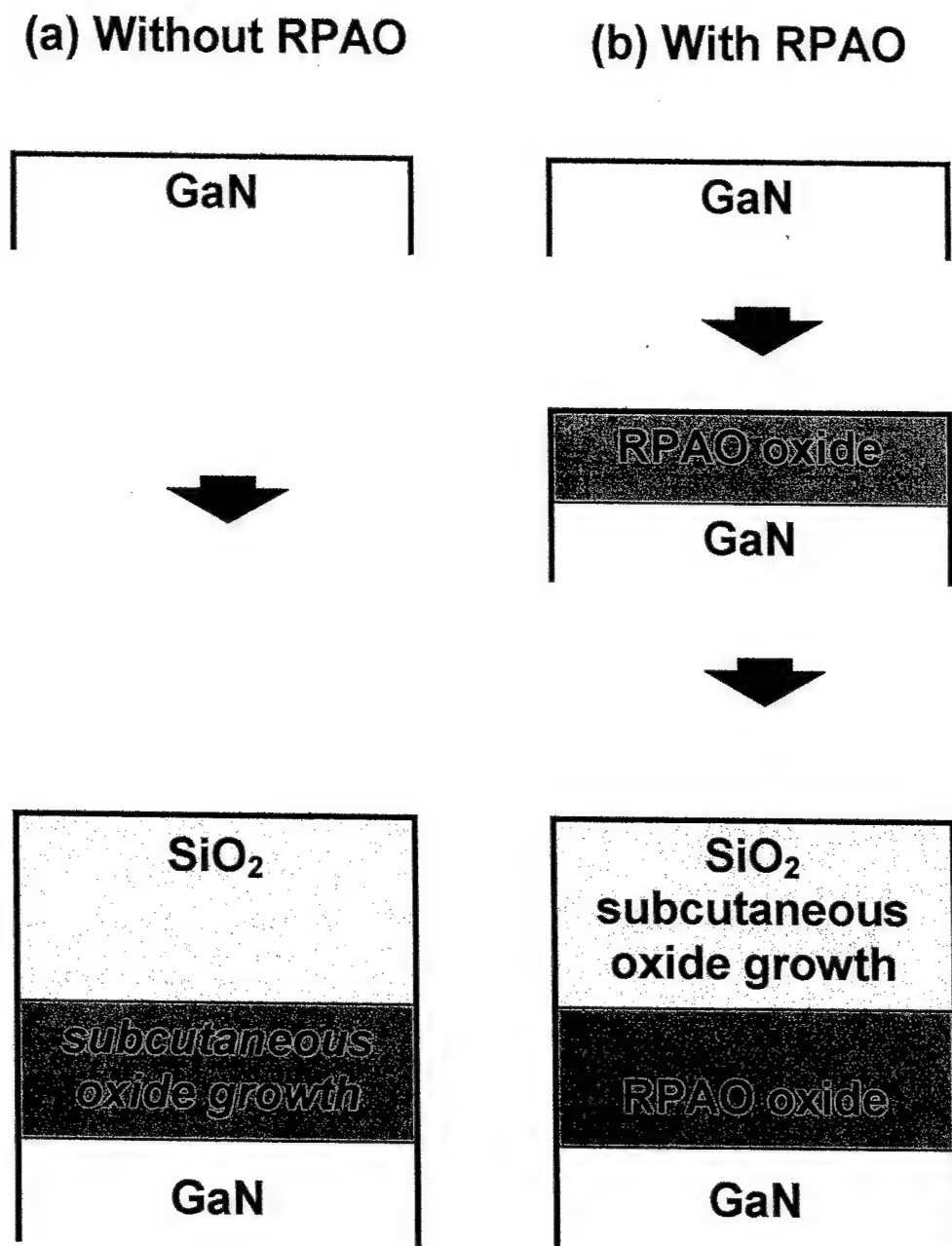


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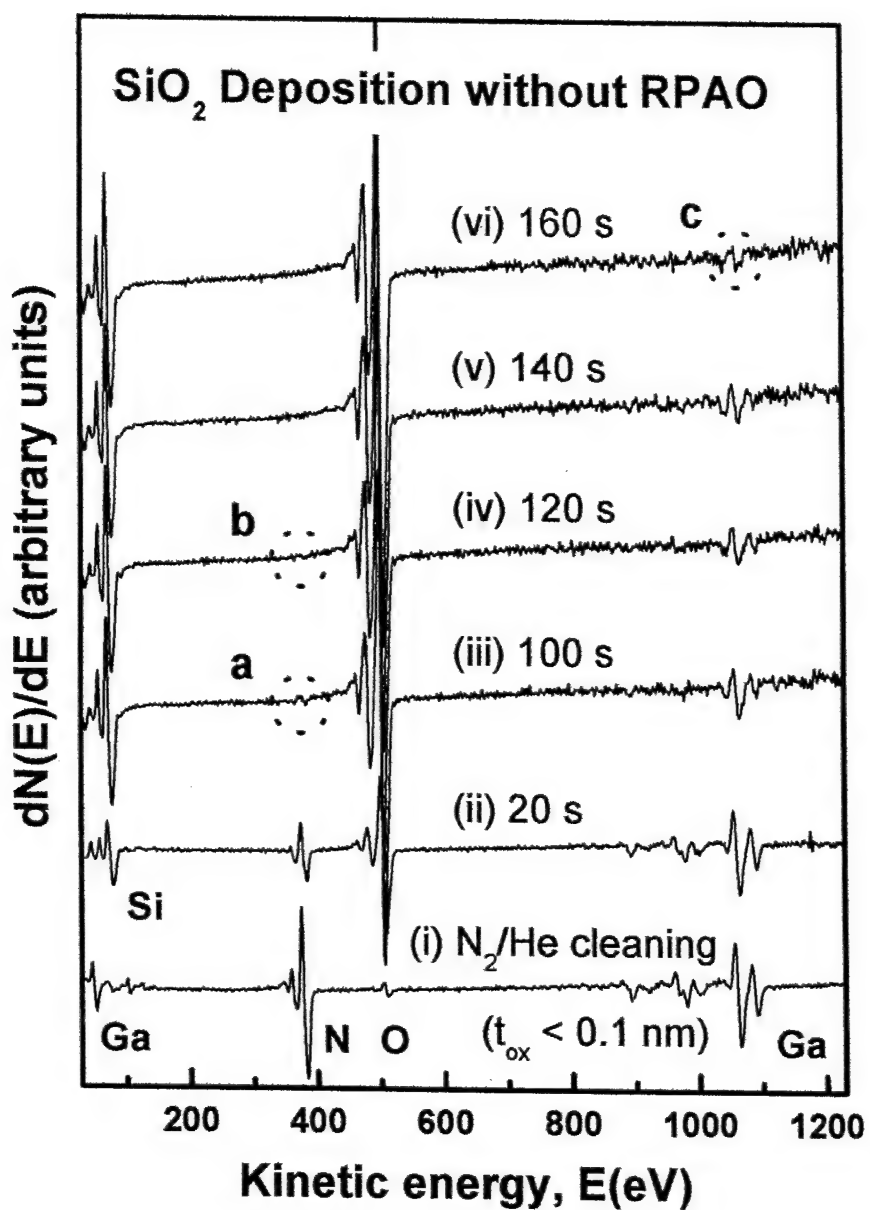


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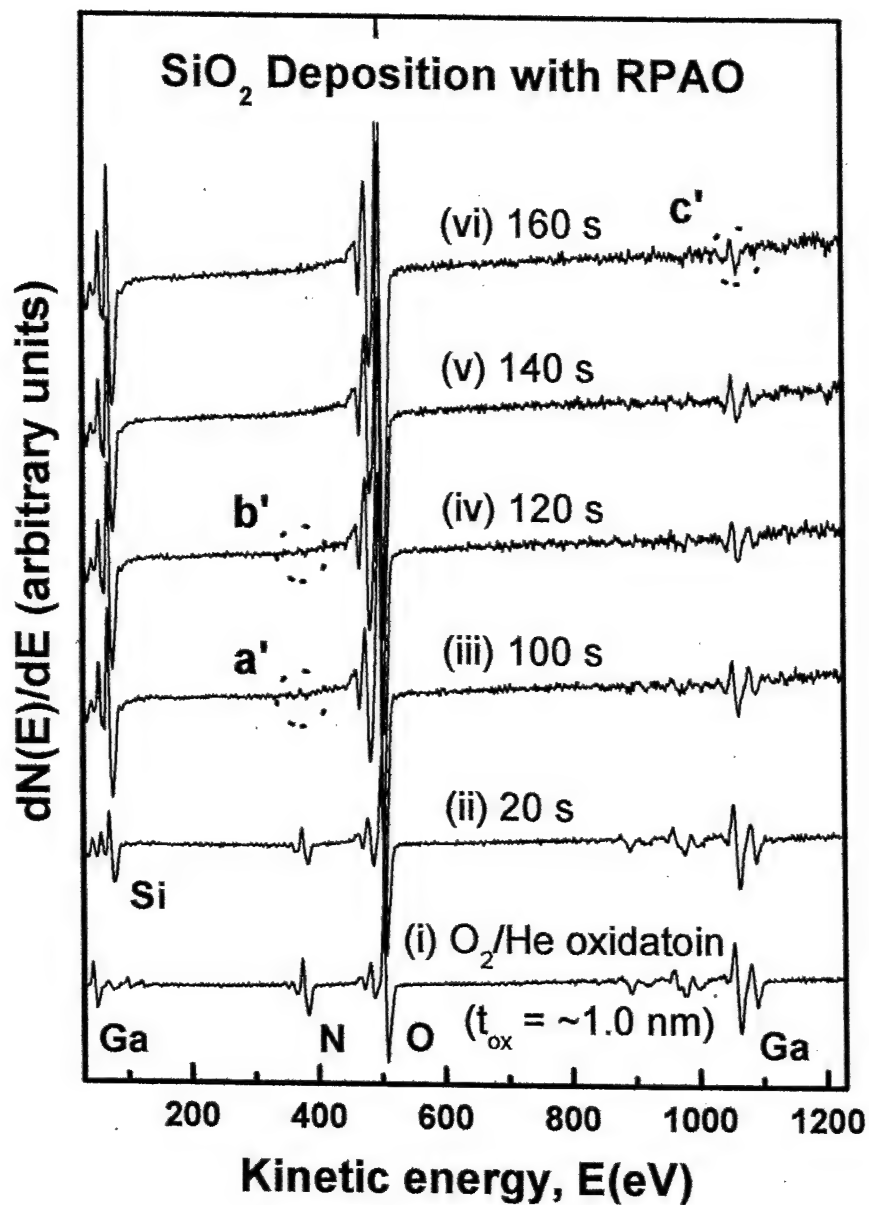


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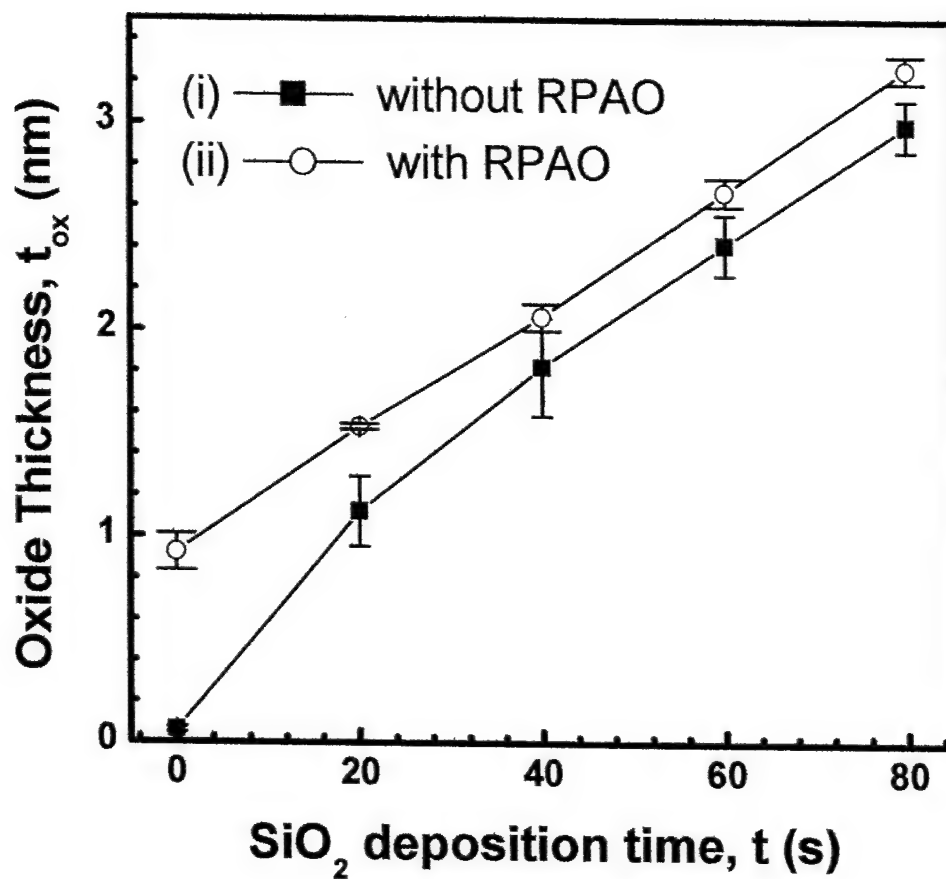


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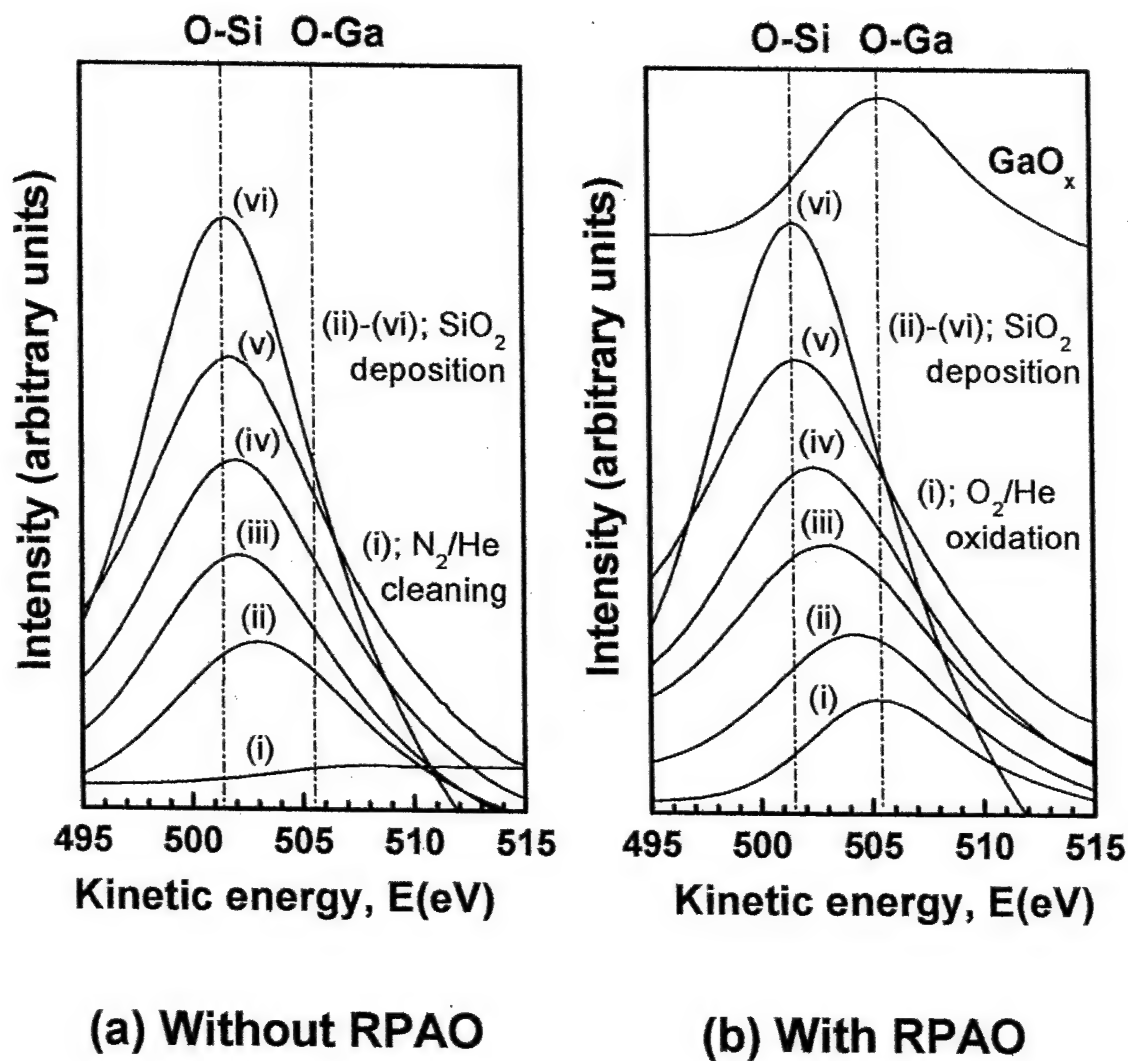


Figure 5 Peak shift of non-differentiated AES spectra by the SiO₂ deposition for (ii) 20, (iii) 40, (iv) 60, (v) 80 and (vi) 180 s on GaN samples (a) without RPAO and (b) with RPAO.

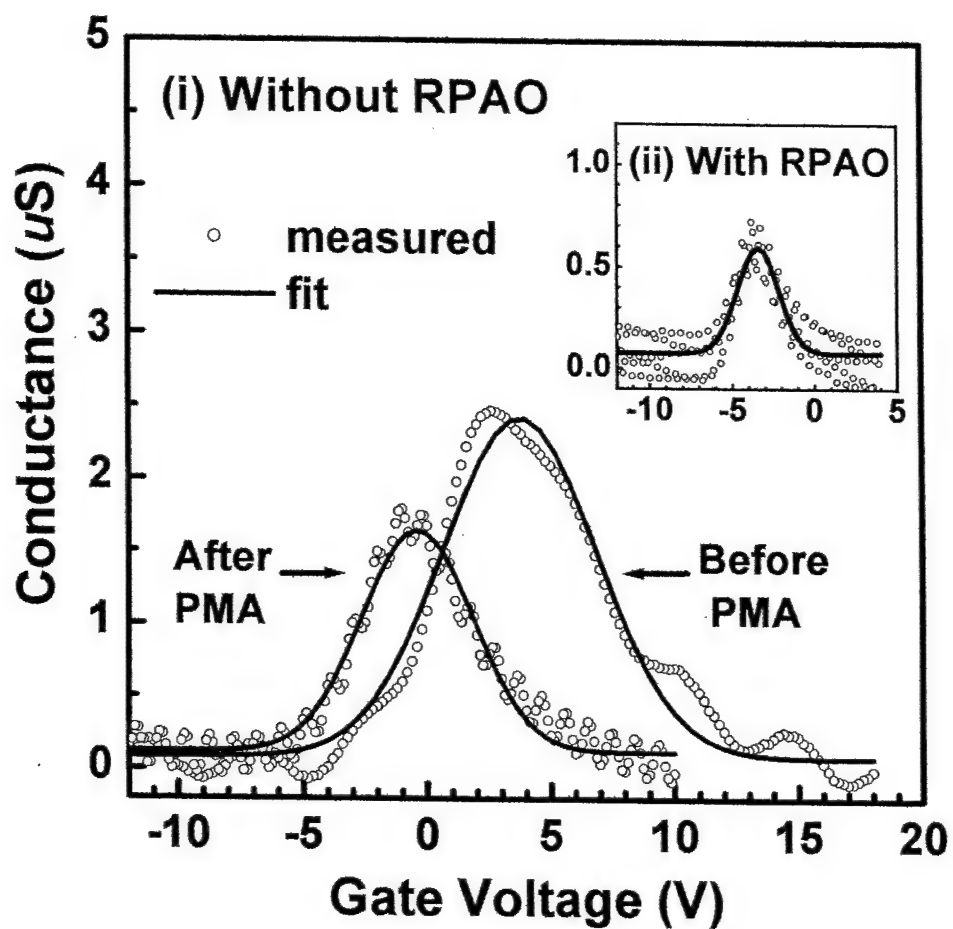


Figure 6 Conductance-voltage (G - V) characteristics of GaN MOS capacitors (i) without RPAO before/after PMA and (ii) with RPAO measured at room temperature and 1 MHz in the dark.

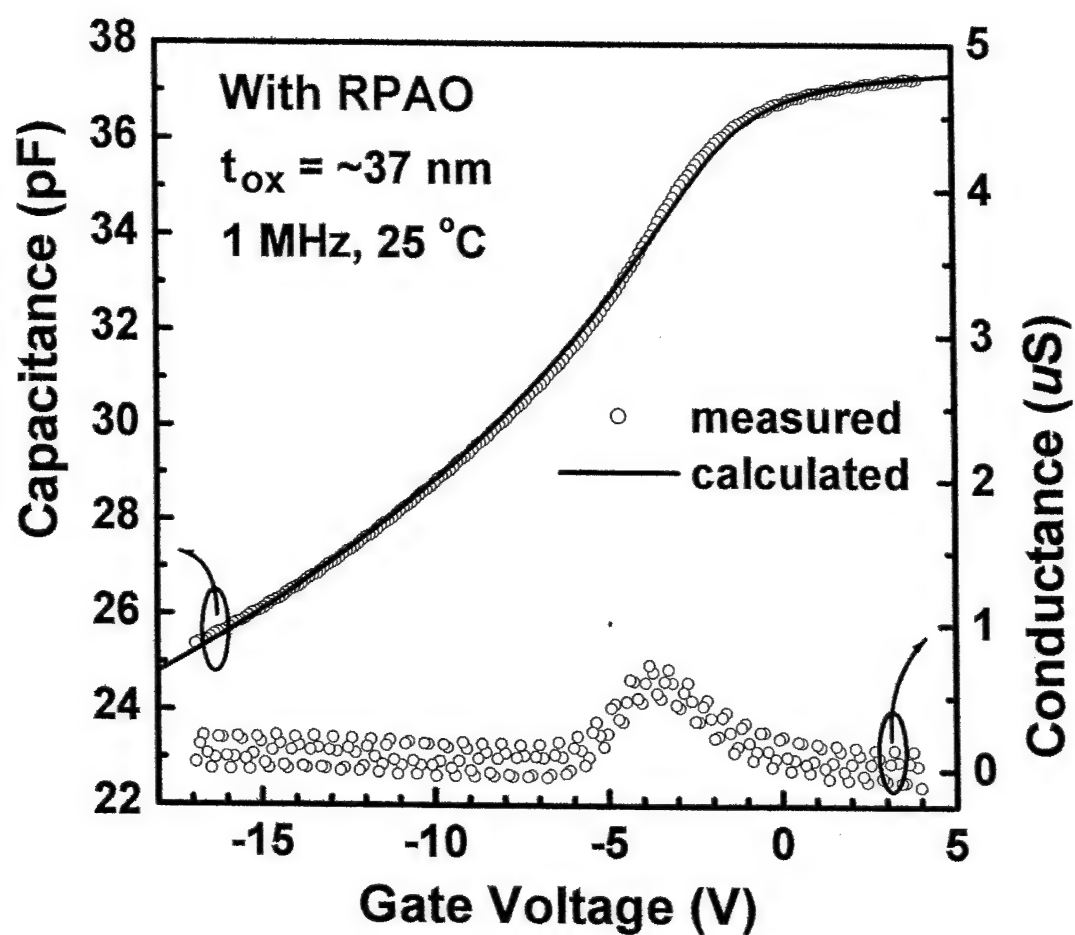


Figure 7 Calculated and measured C - V curve of the GaN capacitor with RPAO at room temperature and 1 MHz. Also shown is the measured conductance.

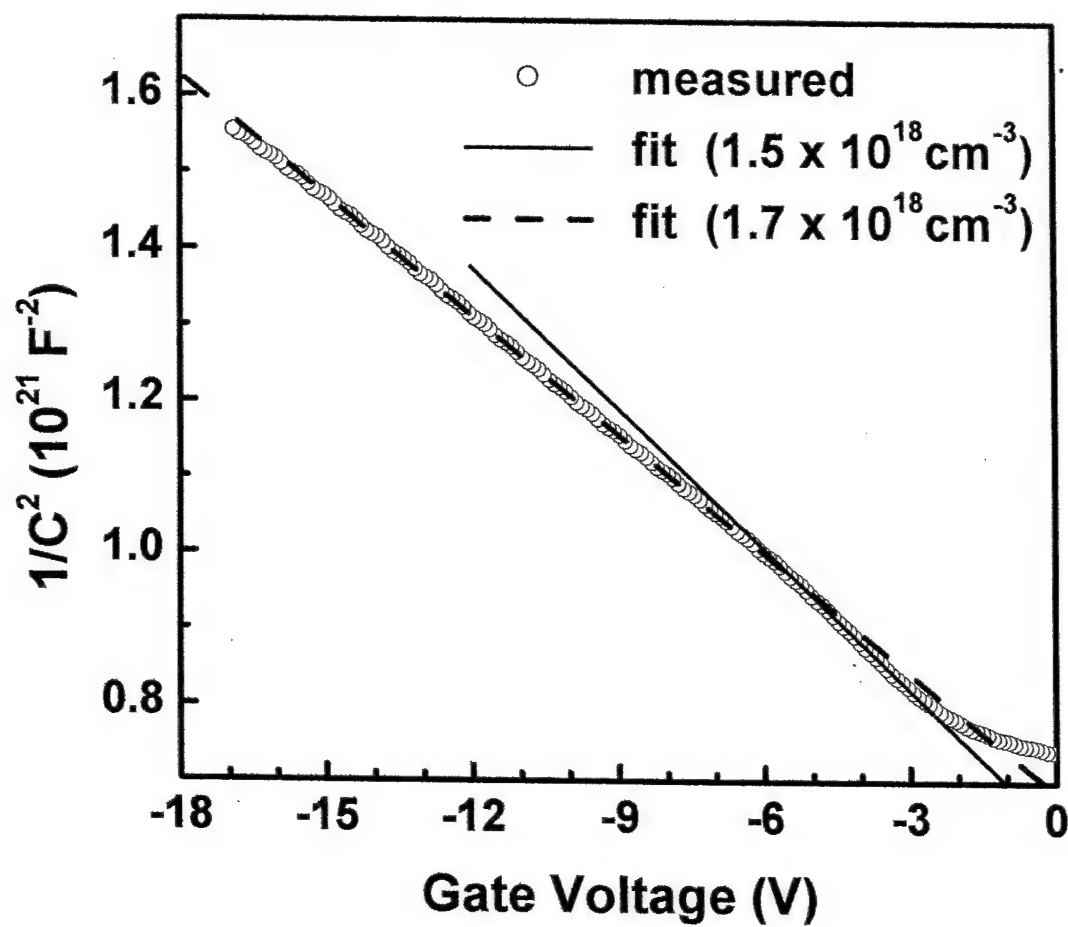


Figure 8 $1/C^2$ characteristics as a function of gate voltage. Net doping concentration (N_D) obtained from the slope was $1.5 \times 10^{18} \text{ cm}^{-3}$ and $1.7 \times 10^{18} \text{ cm}^{-3}$.

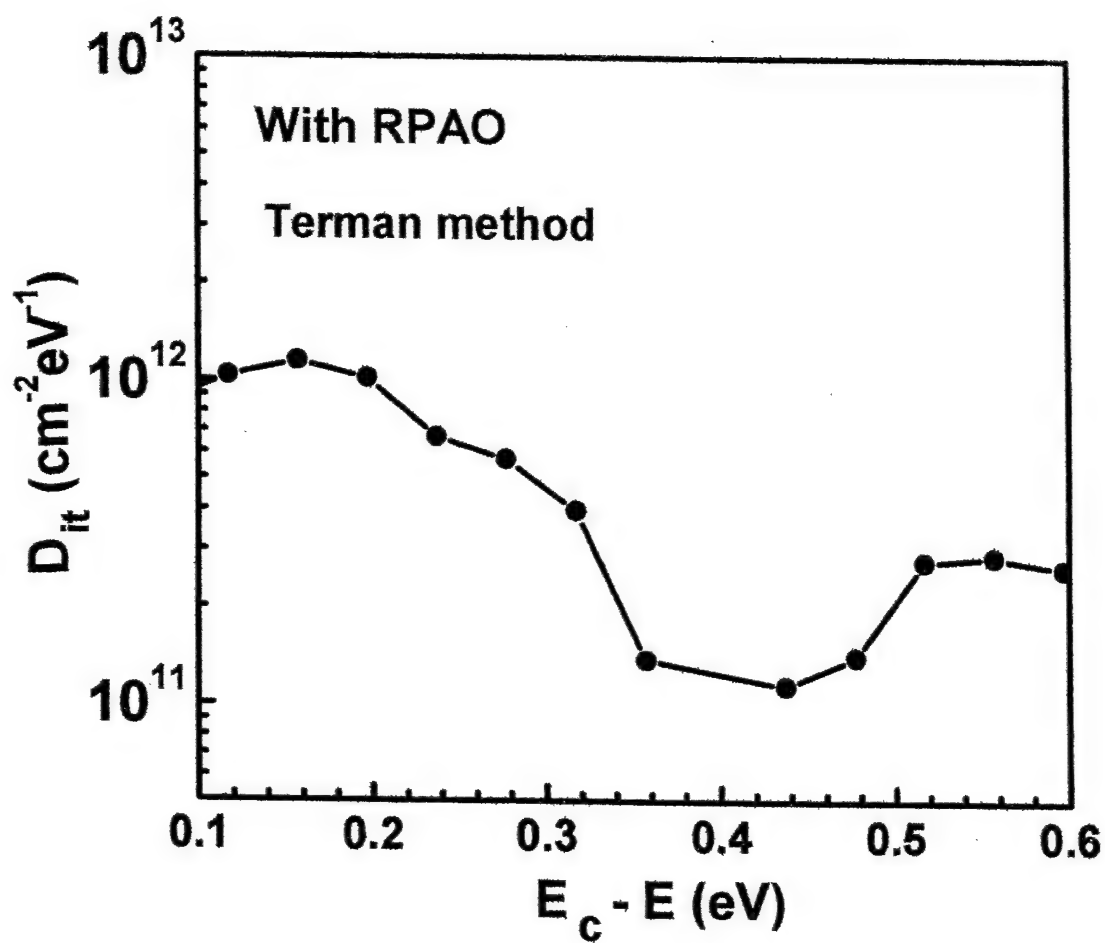


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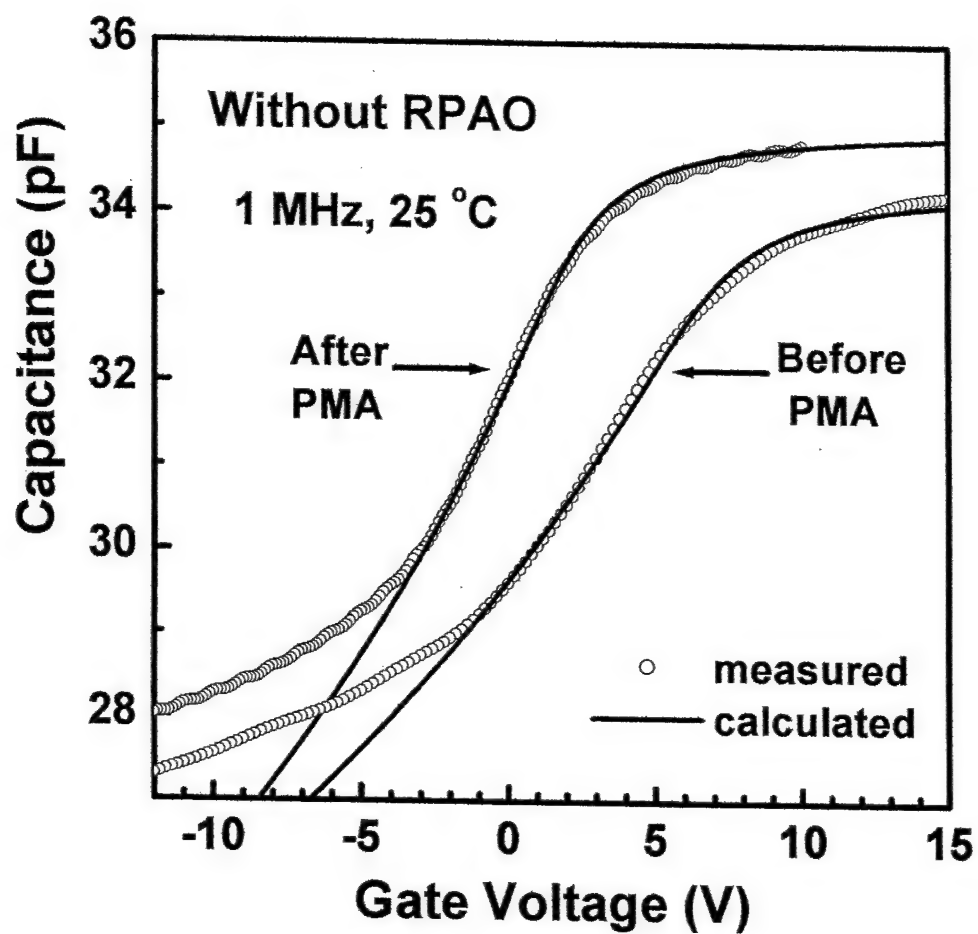


Figure 10 Calculated and measured C - V curve of the GaN capacitors without RPAO before/after PMA at room temperature and 1 MHz.

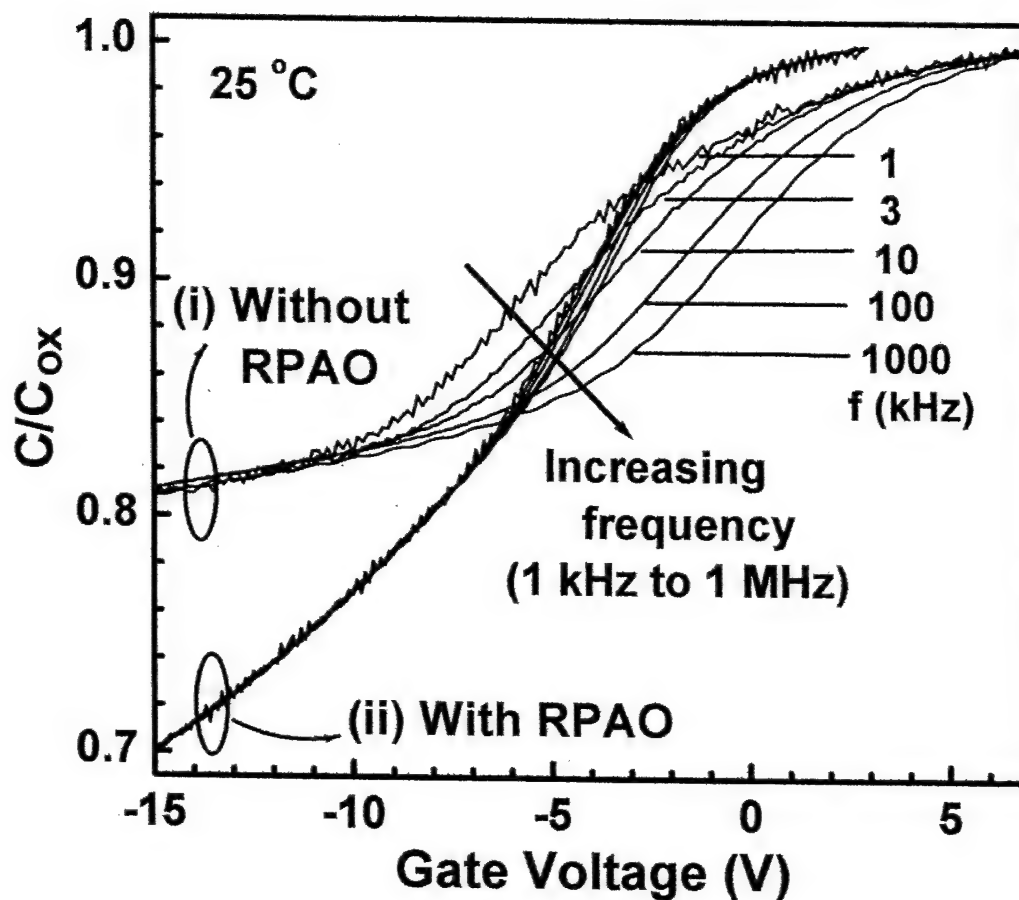


Figure 11 Frequency dependence (1 kHz to 1 MHz) of the C - V characteristics of GaN MOS capacitors (i) without RPAO after PMA and (ii) with RPAO.

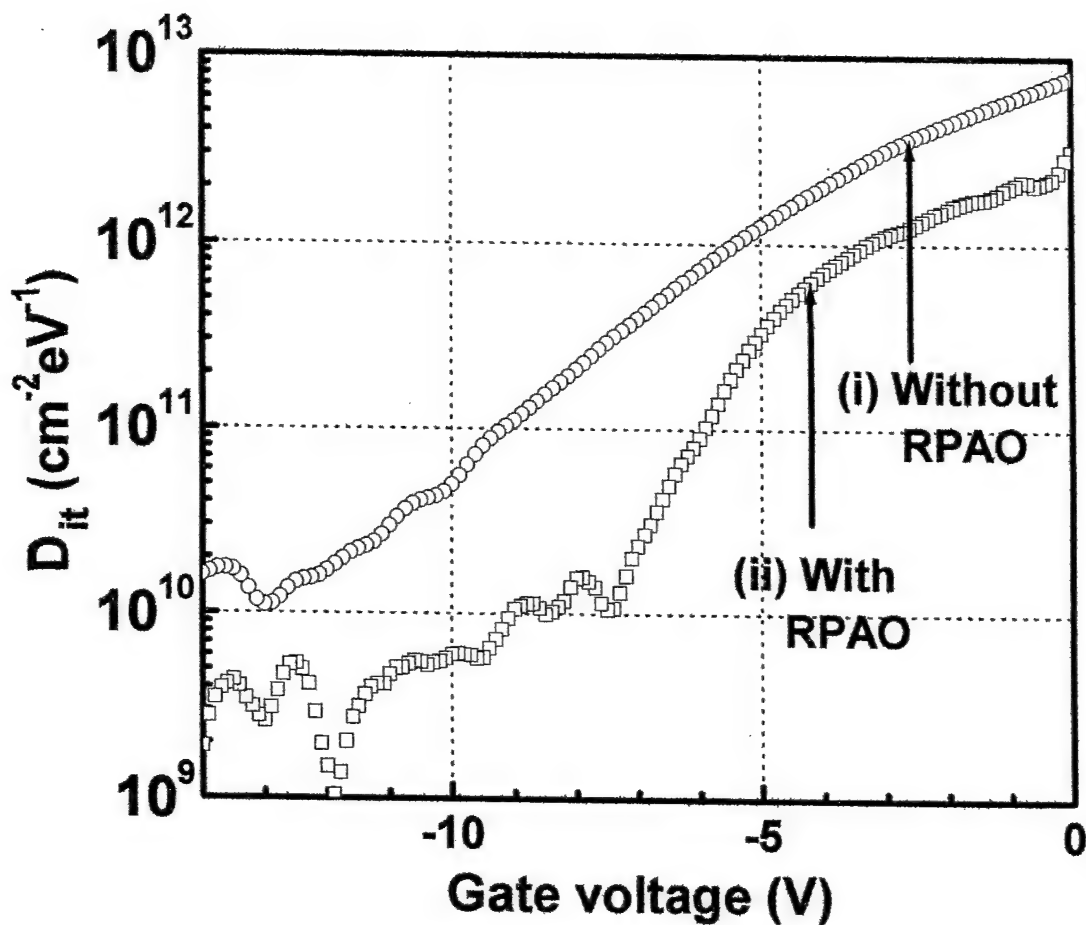


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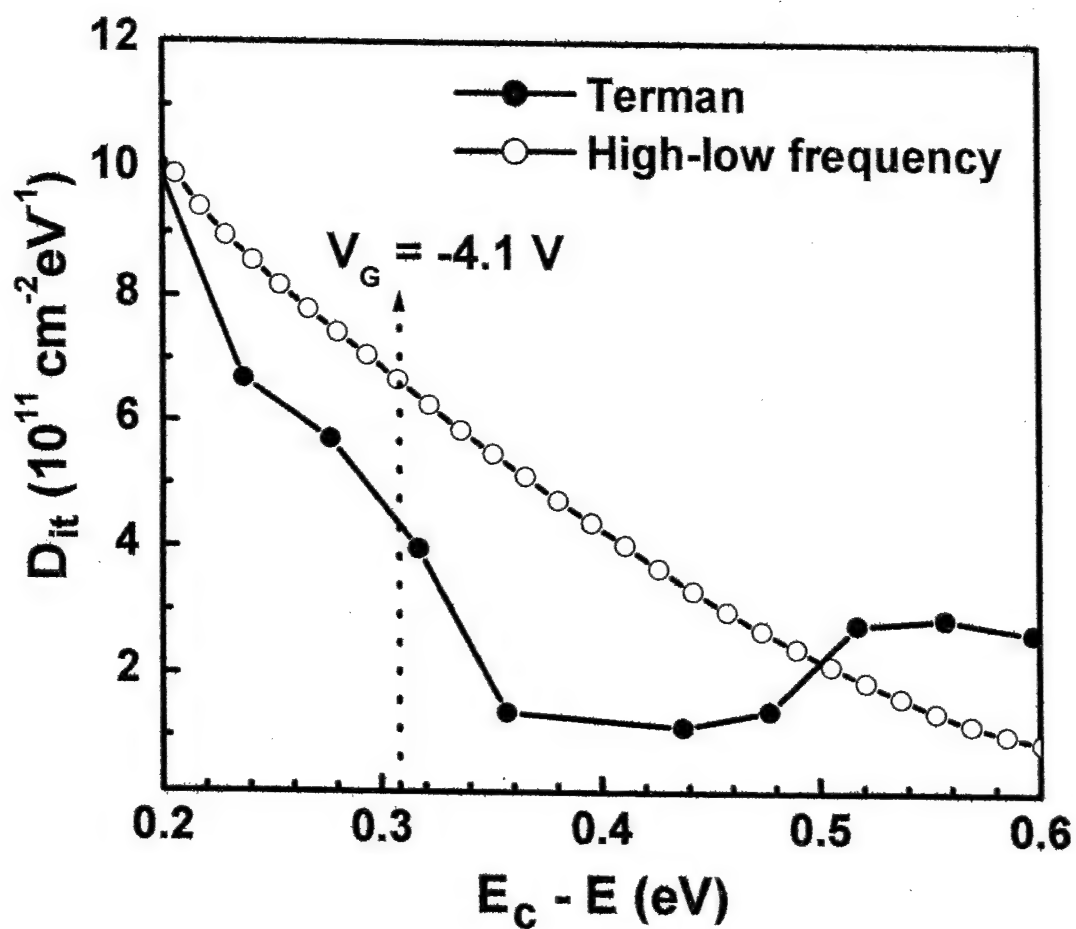


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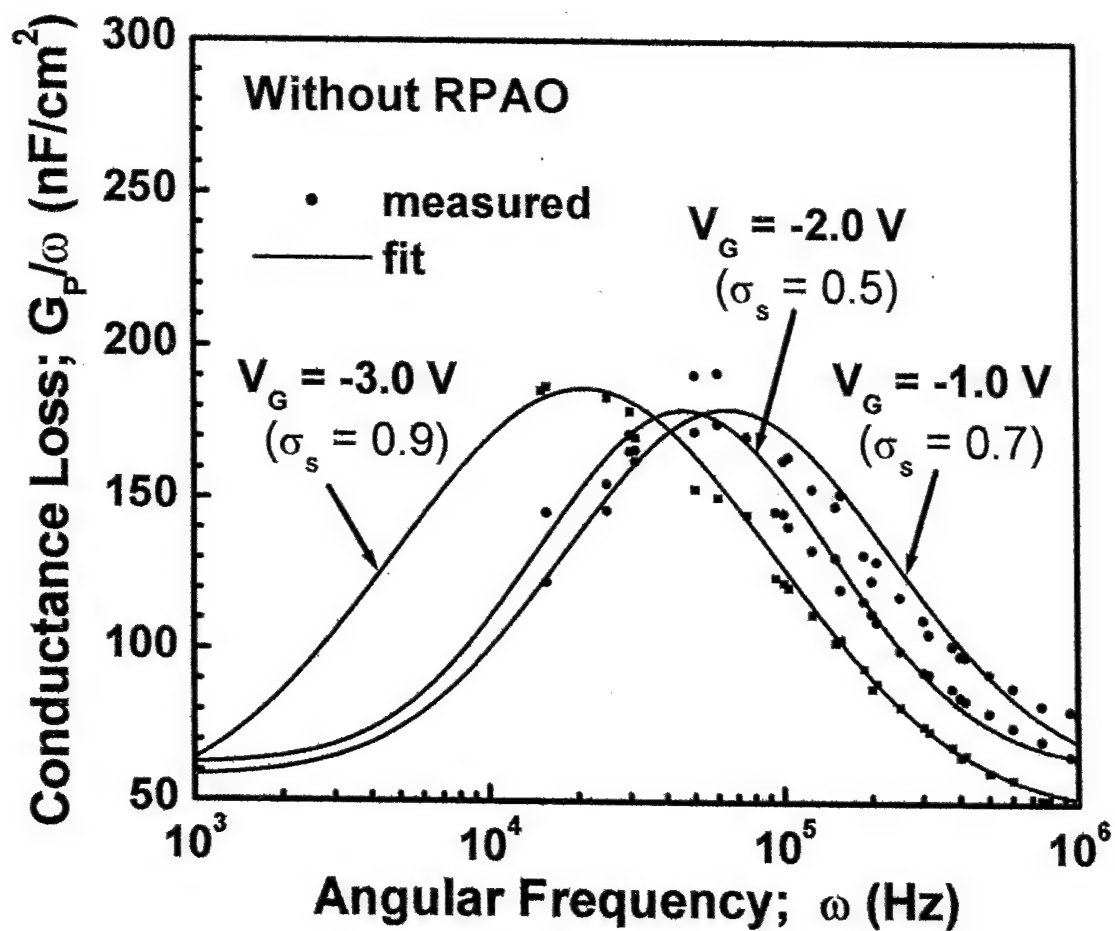


Figure 14 Parallel conductance loss (G_P/ω) versus angular frequency (ω) curves measured at 25 °C for GaN MOS capacitor without RPAO after PMA. The graphically determined standard deviation of band bending (σ_s) was 0.5-0.9 (in the unit of kT/q).

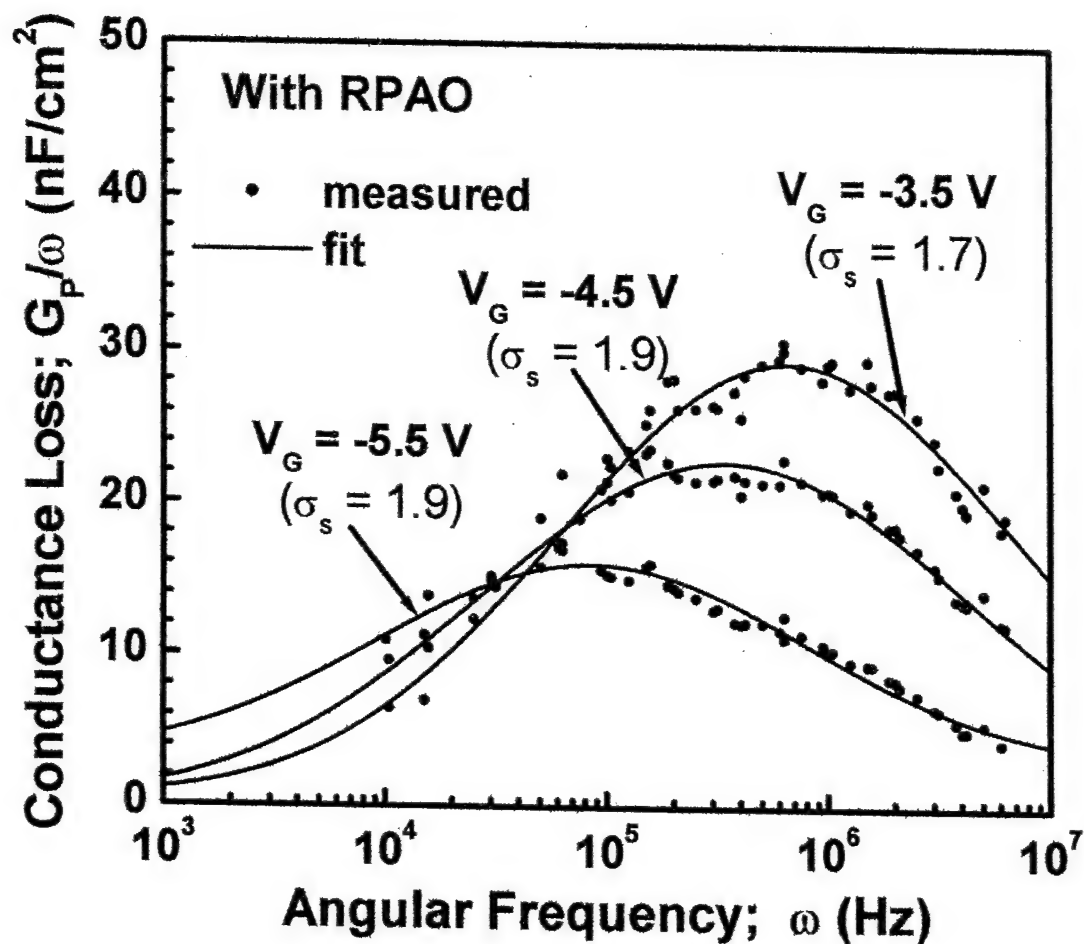


Figure 15 Parallel conductance loss (G_p/ω) versus angular frequency (ω) curves measured at 25 °C for GaN MOS capacitor with RPAO. The graphically determined standard deviation of band bending (σ_s) was 1.7-1.9 (in the unit of kT/q).

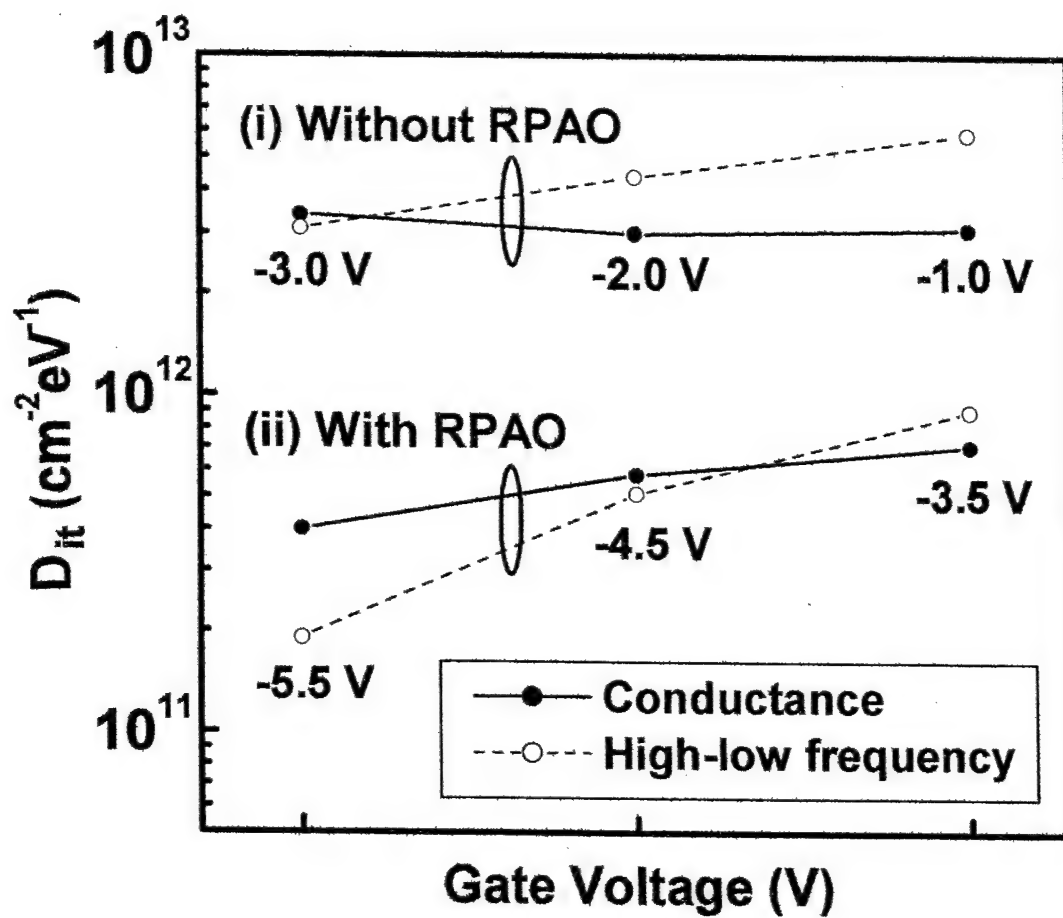


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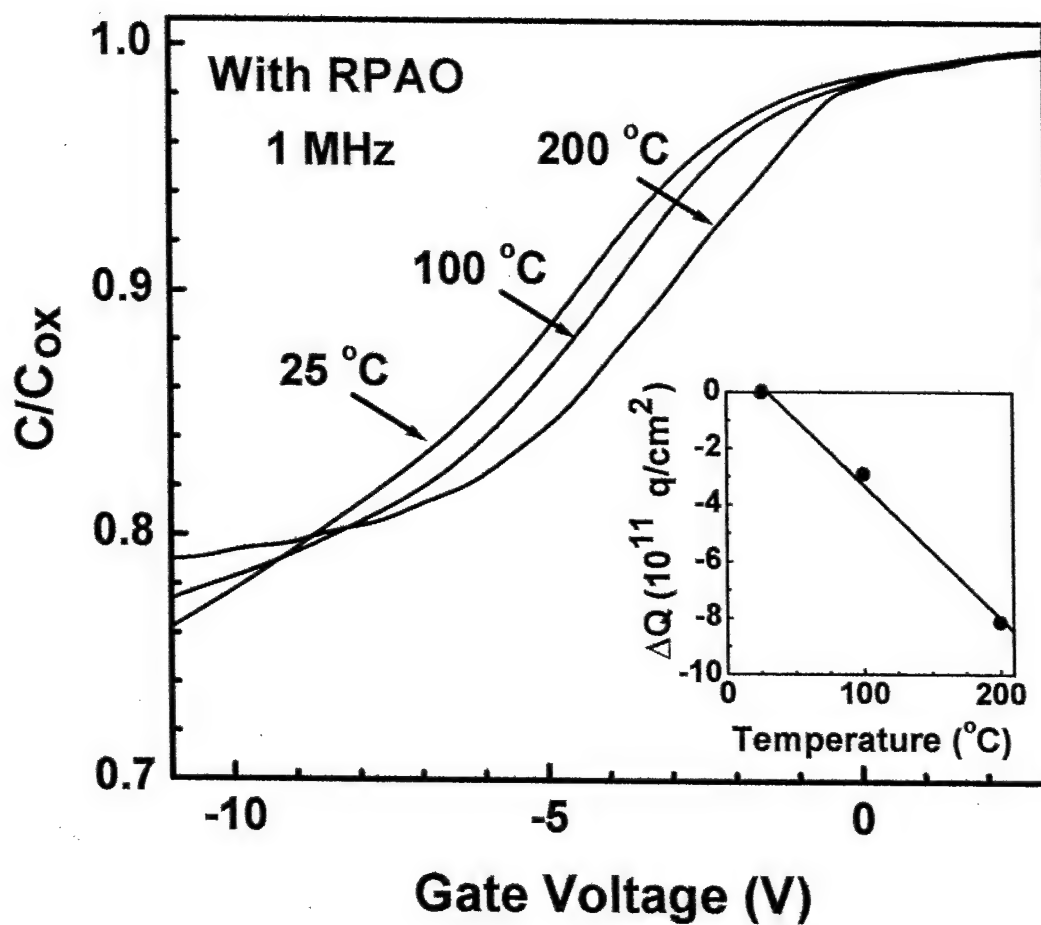


Figure 17 C - V characteristics of GaN MOS capacitors with RPAO measured at 25-200 °C in the dark. Also shown is the change in polarization charge (ΔQ) by increasing temperature [23].

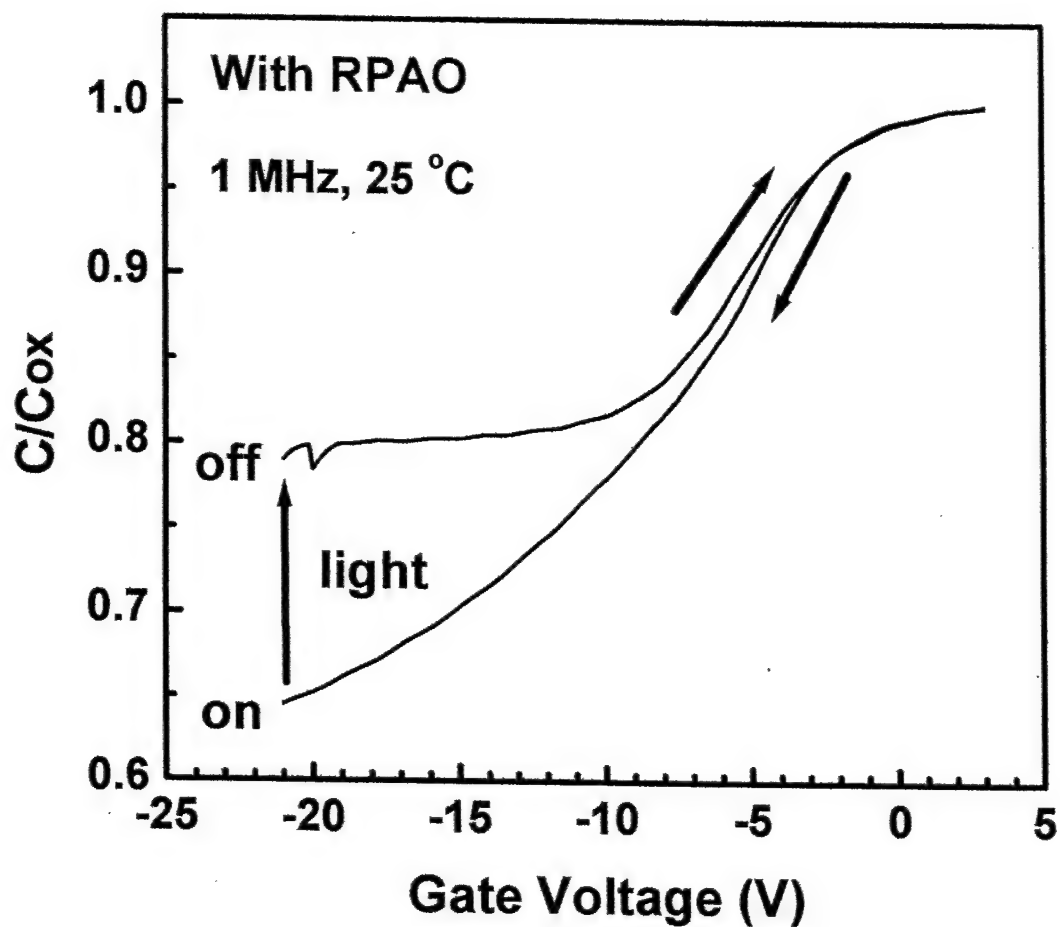


Figure 18
MHz.

Photo-assisted C - V characteristics of GaN MOS capacitors measured at room temperature and 1

Low-Temperature Preparation of GaN-SiO₂ Interfaces with Low Defect Density (II); Remote Plasma-Assisted Oxidation of GaN and Nitrogen Incorporation

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A low temperature remote plasma-assisted oxidation and nitridation processes for interface formation and passivation have been extended from Si and SiC to GaN. The initial oxidation kinetics and chemical composition of thin interfacial oxide were determined from analysis of on-line Auger electron spectroscopy (AES) features associated with Ga, N, and O. The plasma-assisted oxidation process is self-limiting with power law kinetics similar to those for the plasma-assisted oxidation of Si and SiC. Oxidation using O₂/He plasma forms nearly pure GaO_x, and oxidation using 1% N₂O in N₂ forms GaO_xN_y with small nitrogen content, ~4-7 at. %. The quality of interface and dielectric layer was investigated using fabricated GaN metal-oxide-semiconductor (MOS) capacitors. The lowest density of interface states was achieved with a two-step plasma-assisted oxidation and nitridation processes before SiO₂ deposition.

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I INTRODUCTION

GaN has received great attention for applications in optoelectronic and electronic devices due to its direct and wide bandgap properties [1]. Researches of GaN metal-insulator-semiconductor (MIS) system have been focused on reducing the interface state density (D_{it}), and these research efforts can be classified into four groups; i) deposited amorphous SiO₂ [2], Si₃N₄ [3] and high- k Ta₂O₅ [4], ii) epitaxially grown AlN [5], Gd₂O₃ [6] and Ga₂O₃(Gd₂O₃) [7], iii) native oxide by oxidation of GaN surface using thermal [8,9], photoelectrochemical [10-12],

remote O_2/He plasma [13] and N_2O/He plasma methods [14], and iv) gate stacks such as $SiO_2/Si_3N_4/SiO_2$ (ONO) [15].

In previous studies [16,17], device quality Si-SiO₂ interfaces and dielectric bulk film of SiO₂ were prepared using a two-step process: i) remote plasma-assisted oxidation (RPAO) to form a superficially thin interfacial oxide (~0.6 nm) and ii) remote plasma-enhanced chemical vapor deposition (RPECVD) to deposit the SiO₂ film. The same processing steps have been applied to SiC-SiO₂ [18] and GaN-SiO₂ interfaces [13]. This present work is concerned with remote plasma-assisted oxidation of GaN for the independent control of GaN-GaO_x (or GaO_xN_y) interface formation and dielectric film deposition. Three important aspects in preparing thin RPAO oxide, with a composition close to Ga₂O₃ or $x \sim 1.5$, of GaN are (i) RPAO oxide thickness, (ii) RPAO source gas and (iii) incorporated nitrogen content in RPAO oxide. Pure Ga₂O₃ showed high leakage current and did not passivate GaAs [19,20] and SiGe [21] surface due to oxygen vacancies and/or a small amount of reduced Ga in the films. Codeposition of electropositive rare earth elements, like Gd and Y, was suggested for minimizing oxygen vacancies and stabilizing Ga in the fully oxidized 3⁺ states. When the RPAO process is performed to prevent parasitic subcutaneous oxidation of GaN surface which occurs during SiO₂ film deposition [22], RPAO oxide should be carefully controlled as a superficially thin (or several monolayer) oxide. Considering the nitrogen incorporated Si-SiO₂ and Si-high-*k* interface, nitridation of thin RPAO oxide make an important impact on the GaN-GaO_x (or RPAO oxide) interface.

In this study, the RPAO process of GaN surface using O₂, N₂O, and 10 % (or 1 %) N₂O in N₂ source gas has been investigated. The initial oxidation kinetics and chemical composition of thin RPAO oxide were determined from analysis of on-line Auger electron spectroscopy (AES) features associated with Ga, N, and O. Also, remote plasma assisted nitridation of the RPAO oxide is discussed. The quality of interface and dielectric layer was investigated using fabricated GaN metal-oxide-semiconductor (MOS) capacitors.

II. EXPERIMENTAL

The epitaxial GaN (0001) layer was directly grown on the *c*-plane of sapphire by hydride vapor phase epitaxy (HVPE) from TDI. Silicon was used as *n*-type dopant, and the thickness of the GaN epitaxial layer was 5 μm. As grown GaN layer had an electron concentration of 5-10 ×

10^{17} cm^{-3} . As-received 50 mm GaN epi-wafer on sapphire was diced into 4 pieces, and degreased in organic solvents (trichloroethylene, acetone, methanol) each for 10 min. After the wet chemical treatment using 1:1:5 $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ solutions at $\sim 80^\circ\text{C}$ and followed etching in 1:5 $\text{NH}_4\text{OH}:\text{H}_2\text{O}$ solutions at $\sim 80^\circ\text{C}$, GaN samples were loaded into a multi-chamber system [17], which provided a separate remote plasma-assisted process and on-line AES measurement. Prior to the RPAO process, as-loaded GaN sample was exposed to reactive species from a remote N_2/He discharge at 0.02 Torr [22]. Then, the *in situ* cleaned GaN surface was oxidized by the RPAO process at 0.3 Torr using O_2 , N_2O , and N_2O in N_2 source gas. The processing temperature was $250\text{--}300^\circ\text{C}$, and RF power was 30–60 W at 13.56 MHz. For O_2 (or N_2O)/He plasma oxidation, O_2 (or N_2O)/He discharge was used at flows of 20 sccm O_2 (or N_2O) and 200 sccm He. To check for further nitrogen incorporation, GaN samples were exposed to $\text{N}_2\text{O}/\text{N}_2/\text{He}$ plasma using i) 10 % N_2O in N_2 (6/54/200 $\text{N}_2\text{O}:\text{N}_2:\text{He}$) and ii) 1 % N_2O in N_2 (60/200 1 % N_2O in $\text{N}_2:\text{He}$) source gas. For the nitridation process, a thick oxide formed by the RPAO process was exposed to reactive species from a remote N_2/He discharge at 0.3 torr. The processing temperature was 300°C , and RF power was 30 W at 13.56 MHz. The experimental procedure was to alternate AES measurements using 3 keV electron beam with the remote plasma assisted process, i.e., interrupted processing and AES analysis cycles.

For the fabrication of GaN MOS capacitors, the RPAO process was performed on wet chemical treated GaN surface to form an RPAO oxide of ~ 1.0 (or ~ 1.6) nm, and the RPECVD process was performed for 12 min to deposit SiO_2 of ~ 40 nm. After gate dielectric insulator deposition, the sample was rapid-thermal annealed at $\sim 900^\circ\text{C}$ for 30 s in Ar atmosphere. A 300 nm Al layer was evaporated and defined by the conventional lithography process. Post metallization annealing (PMA) was performed at 400°C for 30 min in forming gas (N_2/H_2). The

electrical properties of GaN MOS capacitors were investigated using HP 4284A (precision LCR meter). The area of device under test was $4 \times 10^{-4} \text{ cm}^2$.

III. RESULTS AND DISCUSSION

A. Oxidation rate using on-line AES

The kinetics of the RPAO process on GaN surface are determined by using AES analysis, and thin oxide thickness, t_{ox} (nm) can be fitted by an empirical power-law function of the form, $t_{\text{ox}} = \tau_o t^\beta$, where t is the oxidation time (min), and τ_o and β are fitting parameters. Assuming negligible nitrogen content in the RPAO oxide or GaO_x with $x \sim 1.5$, N *KLL* and O *KLL* AES intensities are given by [23 and reference therein],

$$I_N = I_N^o \exp(-t_{\text{ox}} / \lambda_N) \quad (1)$$

$$I_O = I_O^o [1 - \exp(-t_{\text{ox}} / \lambda_O)] \quad (2)$$

where, I_N = N *KLL* Auger electron intensity from the GaN substrate,

I_N^o = N *KLL* Auger electron intensity from the clean GaN substrate,

λ_N = electron escape depth for N,

I_O = O *KLL* Auger electron intensity from the thin GaO_x layer,

I_O^o = O *KLL* Auger electron intensity from the thick GaO_x layer,

λ_O = electron escape depth for O.

Figure 1 illustrates three samples; (a) clean GaN substrate, (b) thick pure GaO_x , and (c) thin pure GaO_x on GaN substrate. In this study, N_2/He plasma cleaned GaN sample (300°C , 0.02 Torr, 30 W and 15 min) was used as a clean GaN for I_N^o , and O_2/He plasma oxidized GaN sample (300°C , 0.3 Torr, 60 W and 30 min) was used as a thick pure GaO_x for I_O^o , respectively. The obtained value of I_N^o / I_O^o is ~ 0.65 . Figure 2 shows AES spectra from; (i) clean GaN, (ii) thick RPAO oxide and (iii) thin RPAO oxide on GaN substrate. To determine t_{ox} , Eqs. (1) and (2) are combined as the following equation by assigning the same value of electron escape depth, $\lambda = 1.0 \text{ nm}$, for both λ_N and λ_O .

$$t_{ox} = \lambda \ln \left(1 + \frac{I_N^o}{I_O^o} \times \frac{I_O}{I_N} \right) \quad (3)$$

In order to determine t_{ox} only using Eq. (2) without the assumption of negligible nitrogen content in the oxide, I_O in each AES spectra is normalized by the Ga *LMM* Auger electron intensity (I_{Ga}). The normalized intensity of O *KLL* from the thick RPAO oxide layer (I_O^o/I_{Ga}^o) is 2.35. Then, oxide thickness is given by,

$$t_{ox} = -\lambda_O \ln \left(1 - \frac{I_{Ga}^o}{I_O^o} \times \frac{I_O}{I_{Ga}} \right) \quad (4)$$

When the nitrogen content in the RPAO oxide is not negligible, total intensity of N *KLL* (I_N) consists of i) intensity of N *KLL* from the substrate ($I_{N,sub}$) and ii) intensity of N *KLL* from oxide film ($I_{N,filn}$) as shown in Fig. 3. In the initial stage of oxidation, $I_{N,filn}$ is much smaller than $I_{N,sub}$ and can be ignored. As the thickness of oxide film increases, $I_{N,sub}$ gradually reduces and becomes comparable to $I_{N,filn}$. Thus, t_{ox} from Eq. (3) using I_O/I_N becomes smaller than t_{ox} from Eq. (4) using I_O/I_{Ga} .

B. Remote O₂/He plasma oxidation: pure GaO_x/GaN system

Figure 4 shows time evolution of differential AES spectra for the RPAO process of GaN sample using O₂ source gas at 300 °C with plasma power of 30 W. While the Ga *LMM* (~1060.5 eV) feature shows negligible change in strength as the oxidation proceeds, N *KLL* (~377.5 eV) feature which is mainly associated with N-Ga bonding in the GaN substrate decreases in strength, and O *KLL* (~505.5 eV) feature which is mainly associated with O-Ga bonding in the thin oxide layer increases in strength. These changes in relative intensity of N *KLL* and O *KLL* are due to increase of the oxide thickness with time.

Figure 5 shows log-log plots of the oxide thickness versus oxidation time relation for the RPAO process using O₂ gas source at 250 and 300 °C, respectively. The oxide thickness is determined using I_O/I_N . The oxide thickness versus oxidation time relation can be fitted by power law function, $t_{ox} = \tau_o t^\beta$; $t_{ox} = 1.21 t^{0.22}$ (300 °C) and $t_{ox} = 0.74 t^{0.22}$ (250 °C), respectively. The exponential constant, ' β ' of the GaN oxidation (~0.22) is smaller than the corresponding exponential constant for Si (~0.28) [17] and SiC (~0.40) [18]. As shown in Fig. 6, the oxide thickness

using $I_{\text{O}}/I_{\text{Ga}}$ and taking λ_{O} as 1.14 nm, showed good agreement with the oxide thickness using $I_{\text{O}}/I_{\text{N}}$. This suggests that chemical composition of the RPAO oxide using O_2 source gas is nearly pure GaO_x (or GaO_xN_y with negligible y). In addition, the nearly disappeared N *KLL* feature of the GaN sample oxidized at 60 W for 30 min, shown in Fig. 2, also indicates that the nitrogen content in the RPAO oxide is negligible. For this thick oxide sample, the oxide thickness is determined as ~ 3.5 nm. Since the electron escape depth at 400-500 eV is ~ 1.0 nm, theoretically, the oxide thickness using N *KLL* and O *KLL* features can be estimated up to ~ 4.0 nm, in which the AES signal (N *KLL*) from the substrate becomes too weak to be measured. Therefore, power law fitting with an approximation of a homogeneous overlayer/substrate (GaO_x/GaN) system is self-consistent.

Figure 7 displays the peak shift of non-differentiated AES spectra as a function of the oxidation time. As the oxidation proceeds, Ga *LMM* (~ 1060.5 eV) feature gradually shifts to lower energy. The gradual peak shift (~ 1.5 eV) of Ga *LMM* feature indicates Ga-N bonds change to Ga-O bonds. Figure 8 indicates the relative change in composition of oxidized GaN sample as a function of oxidation time, where [Ga], [O] and [N] are Ga, O and N atomic fraction in the film (at. %) [23 and reference therein]. AES intensities of each element are divided by mean free paths to make initial [Ga]/[N] as a unity. Since AES intensities of Ga *LMM* and N *KLL* come from both thin oxide layer and GaN substrate, the determined atomic fractions of each element are not the actual compositions of oxide film until the film grows to the thick film (> 4 nm). Figure 8 only indicates relative concentration changes of each element during oxidation of GaN. Increasing oxidation time, [N] change from ~ 50 (at. %) to near zero (at. %) as [O] change from near zero (at. %) to ~ 50 (at. %), while [Ga] shows negligible change from the initial concentration, ~ 50 (at. %).

C. Remote $\text{N}_2\text{O}/\text{He}$ (or $\text{N}_2/\text{N}_2\text{O}/\text{He}$) plasma oxidation: nitrogen incorporation

To investigate the nitrogen incorporation and possible formation of gallium oxynitride film, GaN samples were exposed to $\text{N}_2\text{O}/\text{He}$ plasma at 300°C with plasma powers of 30 and 60 W, respectively. Figure 9 shows time evolution of differential AES spectra for the RPAO process of GaN sample with 60 W. The changes in relative intensity of N *KLL* and O *KLL* are similar to those of oxidation using O_2 source gas except the slightly remained N *KLL* feature. This indicates that $\text{N}_2\text{O}/\text{He}$ plasma oxidation of GaN surface also resulted in nearly pure GaO_x . The peak shift of non-differentiated AES features from the oxidized GaN sample and the relative change in composition as a function of the oxidation time were similar to the oxidation of GaN using O_2 source gas (not shown in figure).

Figure 10 shows log-log plots of the oxide thickness using $I_{\text{O}}/I_{\text{N}}$ versus the oxidation time and power law fitting for the RPAO process using N_2O source gas at 300 °C with 30 and 60 W, respectively. Oxides thickness using $I_{\text{O}}/I_{\text{N}}$ and fit data from O_2/He plasma oxidation with 30 and 60 W are included as references. In the cases of $t_{\text{ox}} < \sim 2.0$ nm, the growth rate for $\text{N}_2\text{O}/\text{He}$ process decreased as compared to that of the O_2/He plasma process with a similar exponential constant, ' β '. As the t_{ox} increased $> \sim 2.0$ nm, however, the oxidation rate for the N_2O process decreased. The growth rate for the $\text{N}_2\text{O}/\text{He}$ process with 60 W was fitted by two different exponential constants with increasing oxidation time: i) $t_{\text{ox}} = 1.55 t^{0.22}$ up to 3 min and ii) $t_{\text{ox}} = 1.82 t^{0.12}$ for the extended oxidization time. This is attributed to the ignored $I_{\text{N, film}}$ in the determination of oxide thickness using $I_{\text{O}}/I_{\text{N}}$, and also indicates that small amount of nitrogen was incorporated into the RPAO oxide layer.

Figure 11 show log-log plots of the oxide thickness versus the oxidation time for the RPAO process using i) 10 % N_2O and ii) 1 % N_2O source gas, respectively. Oxide thickness was determined using $I_{\text{O}}/I_{\text{N}}$ and using $I_{\text{O}}/I_{\text{Ga}}$, respectively. Power law fitting was performed for the oxide thickness using $I_{\text{O}}/I_{\text{Ga}}$. When t_{ox} increased $> \sim 2.0$ nm, the oxide thickness using $I_{\text{O}}/I_{\text{N}}$ shows deviation from the power law fitting. This deviation confirms the nitrogen incorporation in the RPAO oxide layer, but indicates that the nitrogen incorporation was not significantly enhanced by increasing N/O ratio in source gas. Figure 12 shows the relative change in composition of oxidized GaN sample as a function of oxidation time. For the oxidized sample using 10 % N_2O for 120 min, the value of [N], ~ 4 at. %, is mainly obtained from the oxide layer because the oxide thickness is $> \sim 3.5$ nm. For the sample using 1% N_2O for 180 min, AES intensities of N *KLL* from the GaN substrate is not negligible yet. Thus, the incorporated nitrogen content in the sample using 1 % N_2O will be ~ 4 -7 at. %. Although other characterization methods need to obtain exact value of incorporated nitrogen content, the present result indicates that only small amount of nitrogen was incorporated in the oxide during RPAO process in the studied ranges of N/O in source gas.

D. Remote N_2/He plasma nitridation of GaO_x : enhanced nitrogen incorporation

Figure 13 shows differential AES spectra for (i) the thick RPAO oxide (> 3.5 nm) film prepared from O_2/He plasma oxidation of the GaN followed by (ii) – (vi) the exposure to N_2/He plasma for 5-150 min at 0.3 Torr. The intensity of N *KLL* increased as the exposure time to N_2/He plasma increased to 5-90 min, and saturated with no significant spectral change for the extended nitridation time. By reoxidation using O_2/He plasma for 1 min, this increased intensity of N *KLL* feature reduced to the initial values of the RPAO oxide film before the exposure to N_2/He plasma. Figure 14 displays the non-differentiated AES features of a GaN sample. As the exposure time to

N_2/He plasma increased, Ga *LMM* (~ 1058.5 eV) and O *KLL* (~ 505.0 eV) features of oxide film gradually shifts to higher energy. Figure 15 shows the atomic fractions of each element, [Ga], [O] and [N]. While [Ga] shows negligible change from the initial concentration of ~ 50 (at. %), [N] and [O] saturate to ~ 25 (at. %) with increasing nitridation time.

E. Interface quality of GaN MOS system

The impacts of RPAO oxide thickness and nitrogen incorporation on the quality of interface and dielectric layer were investigated using test GaN MOS capacitors. From the oxide thickness-oxidation time relation shown in Fig. 5, the RPAO process using O_2 source gas was performed for 30 s (or 180 s) to obtain a thin RPAO oxide of ~ 1.0 nm (or ~ 1.6 nm). For the nitrogen incorporated RPAO oxide, GaN MOS samples were prepared by (i) the RPAO process using 1% N_2O in N_2 source gas and (ii) the RPAO process using O_2 source gas followed by nitridation using N_2/He plasma at 0.3 Torr for 90 s, respectively. To control the thickness of RPAO oxide using 1% N_2O in N_2 source gas as ~ 1 nm, the RPAO process performed for 600 s as shown in Fig. 11. In this section, the characterizations of each GaN MOS samples were focused on interface trapped charge (Q_{it}) rather than oxide fixed charge (Q_f) because the extraction of Q_f from the flat band voltage shift (ΔV_{fb}) has several uncertainties such as (i) compensated effect [24] between Q_f and Q_{it} and (ii) uncertain doping concentration of GaN MOS system which was usually obtained from close fit of the capacitance-voltage ($C-V$) curve. The exact evaluation of Q_f using ΔV_{fb} can be possible after minimizing Q_{it} .

Figure 16 and 17 show the frequency dependence of $C-V$ characteristics of GaN MOS capacitors. The gate voltage was swept from positive to negative voltage at room temperature in the dark, and frequencies were 3 kHz, 10 kHz, 100 kHz and 1 MHz. To determine D_{it} of each GaN MOS sample, high-low frequency method was applied to measured $C-V$ curves. $C-V$ curves measured at 1 MHz and 3 kHz were used as high and low frequency $C-V$ curves, respectively.

The minimum D_{it} of each GaN MOS capacitor was determined at the gate voltage where measured $C-V$ curves at 3 kHz and 1 Mhz showed the maximum capacitance difference (ΔC_{max}). Note that the actual D_{it} will be higher than estimated value using this method. Using the $C-V$ curves at 3 kHz and 1 MHz, D_{it} is calculated from [25]

$$D_{it} = \frac{C_{ox}}{q} \left(\frac{C_{if}/C_{ox}}{1 - C_{if}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \quad (5)$$

Figure 18 shows minimum D_{it} of each GaN MOS capacitor determined at the gate voltage of ΔC_{max} . By increasing the thickness of RPAO oxide from (i) ~ 1.0 to (ii) ~ 1.6 nm, D_{it} increased from $\sim 6 \times 10^{11}$ to $9 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Considering the sample using 1% N_2O in N_2 source gas performed for 600 s, it is reasonable that this increased D_{it} is caused by the increased thickness of RPAO oxide rather than possible plasma-induced damage. The lowest value of D_{it} , $\sim 4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, was obtained by the RPAO process using O_2 source gas with followed nitridation using N_2/He plasma.

IV. CONCLUSION

Remote plasma assisted oxidation of GaN surface using O_2 , N_2O , and 10 % (or 1 %) N_2O in N_2 source gas has been investigated as the first step for the independent control of GaN- GaO_x (or GaO_xN_y) interface formation and dielectric film deposition. The initial oxidation kinetics and chemical composition of thin oxide are determined from analysis of on-line AES features associated with Ga, N and O. The plasma-assisted oxidation process is self-limiting with power law kinetics similar to those for the plasma-assisted oxidation of Si and SiC. Oxidation using O_2/He plasma forms nearly pure GaO_x and oxidation using 1% N_2O in N_2 forms GaO_xN_y with small nitrogen content, ~ 4 -7 at. %. The impacts of RPAO oxide thickness and nitrogen incorporation on the quality of interface and dielectric layer were investigated, and the lowest value of interface state density, $\sim 4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, was obtained by the

RPAO process using O_2 source gas to form ~ 1.0 nm of RPAO oxide and followed by nitridation using N_2/He plasma. The control of RPAO oxide as a superficially thin (or several monolayer) oxide and enhancement of incorporated nitrogen content are essential requirements to reduce interface state density of GaN MOS systems.

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Figure captions

Figure 1 Schematic representation of three samples; (a) clean GaN substrate, (b) thick pure GaO_x and (c) thin pure GaO_x on GaN substrate. I_N° (or I_N) is N *KLL* Auger electron intensity from the clean GaN substrate (or from the GaN substrate with thin oxide). I_O° (or I_O) is O *KLL* Auger electron intensity from the thick GaO_x layer (or from the thin GaO_x layer).

Figure 2 Differential AES spectra from (i) clean GaN, (ii) thick RPAO oxide and (iii) thin RPAO oxide on GaN substrate. N_2/He plasma cleaned GaN sample (300 °C, 0.02 Torr, 30 W and 15 min) was used as a reference sample for a clean GaN, and O_2/He plasma oxidized GaN sample (300 °C, 0.3 Torr, 60 W and 30 min) was used as a reference sample for a thick pure GaO_x .

Figure 3 Schematic representation of thin RPAO oxide, or GaO_xN_y , with non-negligible nitrogen content, on GaN substrate. When the nitrogen content in the oxide does not negligible, total intensity of N *KLL* (I_N) consists of i) intensity of N *KLL* from the substrate ($I_{N, \text{sub}}$) and ii) intensity of N *KLL* from oxide film ($I_{N, \text{film}}$).

Figure 4 Time evolution of differential AES spectra from (i) N_2/He plasma cleaned GaN sample and (ii)-(vi) O_2/He plasma oxidation processing of GaN surface for 0.5 to 30 min.

Figure 5 Log-log plots of the oxide thickness (t_{ox}) as a function of oxidation time (t) for the RPAO process using O_2 source gas at 250 and 300 °C, respectively. The straight lines connecting the data points represent a power-law dependence, i.e., $t_{\text{ox}} = \tau_o t^\beta$, where τ_o and β are fitting parameters. The oxide thickness is determined from Eq. (3) using I_O/I_N with an assumption of a homogeneous overlayer/substrate (GaO_x/GaN) system.

Figure 6 Log-log plots of the oxide thickness (t_{ox}), determined from Eq. (4) using I_O/I_{Ga} and taking λ_O as 1.14 nm, as a function of oxidation time (t) for the same RPAO process shown in Fig. 5. The oxide thickness and fitting data shown in Fig. 5 are also included as references.

Figure 7 Time evolution of non-differential AES spectra from in-situ N_2/He plasma cleaned GaN sample and O_2/He plasma oxidation processing of GaN surface for 0.25 to 60 min.

Figure 8 Relative change in composition of GaO_x as a function of nitridation time, where, $[\text{Ga}]$, $[\text{O}]$ and $[\text{N}]$ are Ga, O and N atomic fraction in the film (at. %).

Figure 9 Time evolution of differential AES spectra from (i) N_2/He plasma cleaned GaN sample and (ii)-(vii) $\text{N}_2\text{O}/\text{He}$ plasma oxidation processing of GaN surface for 0.5 to 60 min. The notation (20/200) in the figure refers to the flow rates of N_2O and He, respectively, in units of standard cubic centimeters per second (sccm).

Figure 10 Log-log plots of the oxide thickness (t_{ox}) as a function of oxidation time (t) for the RPAO process using N_2O source gas at 300 °C with 30 and 60 W, respectively. The oxide

thickness is determined from Eq. (3) using I_O/I_N . The oxide thickness and fitting data using O_2 source gas are also included as references.

Figure 11 Log-log plots of the oxide thickness (t_{ox}), determined from Eq. (4) using I_O/I_{Ga} and taking λ_O as 1.14 nm as a function of oxidation time (t). The notation 10 % and 1 % in the figure refer to 10 % N_2O in N_2 and 1 % N_2O in N_2 .

Figure 12 Relative change in composition of oxidized GaN sample as a function of oxidation time, where, [Ga], [O] and [N] are Ga, O and N atomic fraction in the film (at. %).

Figure 13 Time evolution of differential AES spectra from (i) O_2/He plasma oxidized GaN sample (GaO_x , ~3.5 nm) and (ii)-(vi) N_2/He plasma nitridation processing of GaO_x for 5 to 150 min.

Figure 14 Time evolution of non-differential AES spectra from O_2/He plasma oxidized GaN sample (GaO_x , ~3.5 nm) and N_2/He plasma nitridation processing of GaO_x .

Figure 15 Relative change in composition of GaO_x as a function of nitridation time, where, [Ga], [O] and [N] are Ga, O and N atomic fraction in the film (at. %).

Figure 16 Frequency dependence (3 kHz, 10 kHz, 100 kHz, and 1 MHz) of the $C-V$ characteristics of GaN MOS capacitors. The RPAO process using O_2 source gas was performed for (a) 30 s to obtain thin RPAO oxide of ~1.0 nm and (b) 180 s to obtain thin RPAO oxide of ~1.6 nm. The minimum D_{it} of each GaN MOS capacitor was determined at the gate voltage where measured $C-V$ curves at 3 kHz and 1 Mhz showed the maximum capacitance difference (ΔC_{max}).

Figure 17 Frequency dependence (3 kHz, 10 kHz, 100 kHz, and 1 MHz) of the $C-V$ characteristics of GaN MOS capacitors. (a) the RPAO process using 1% N_2O in N_2 source gas and (b) the RPAO process using O_2 source gas with followed nitridation using N_2/He plasma.

Figure 18 Minimum density of interface state (D_{it}) of GaN MOS capacitors with RPAO process using (i) O_2 source gas for 30 s, (ii) O_2 source gas for 180 s, (iii) 1% N_2O in N_2 source gas for 600 s and (iv) O_2 source gas for 30 s with followed nitridation using N_2/He plasma for 90 s.

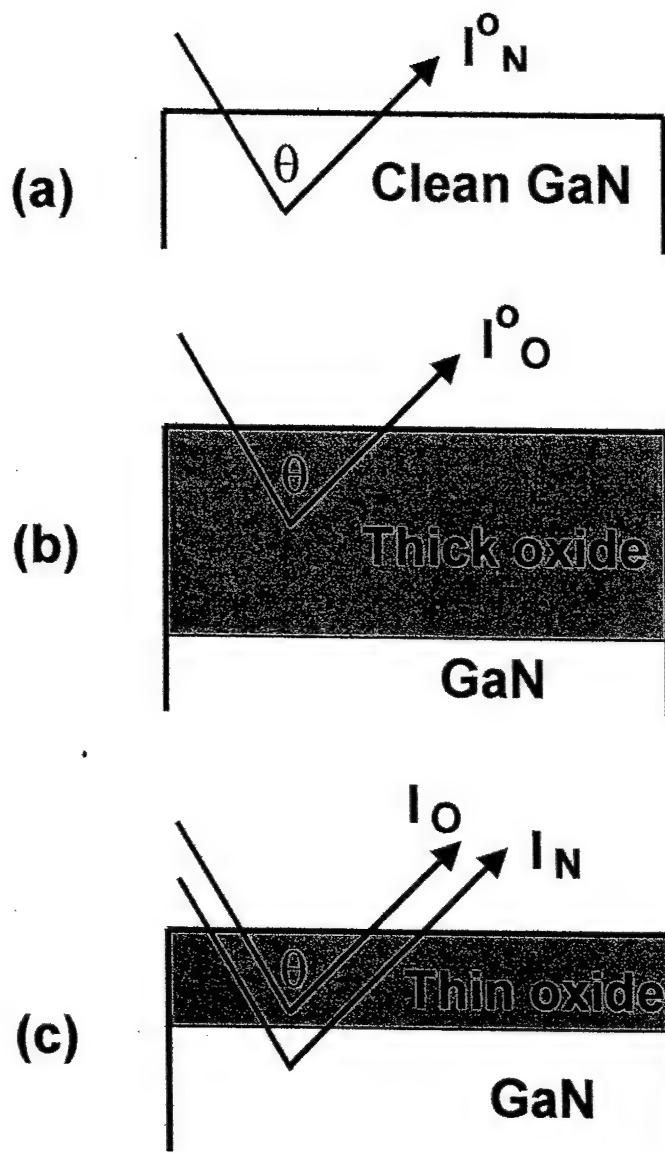


Figure 1 Schematic representation of three samples; (a) clean GaN substrate, (b) thick pure GaO_x and (c) thin pure GaO_x on GaN substrate. I_N^0 (or I_N) is N *KLL* Auger electron intensity from the clean GaN substrate (or from the GaN substrate with thin oxide). I_O^0 (or I_O) is O *KLL* Auger electron intensity from the thick GaO_x layer (or from the thin GaO_x layer).

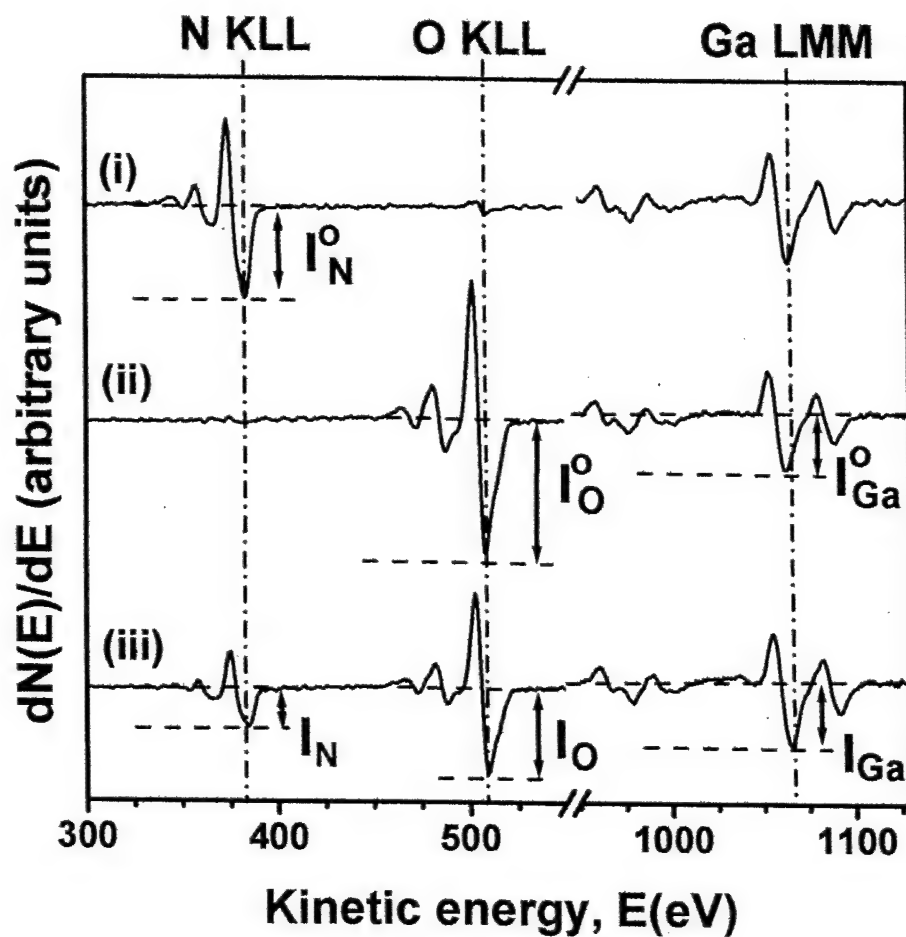


Figure 2 Differential AES spectra from (i) clean GaN, (ii) thick RPAO oxide and (iii) thin RPAO oxide on GaN substrate. N_2/He plasma cleaned GaN sample ($300^\circ C$, 0.02 Torr, 30 W and 15 min) was used as a reference sample for a clean GaN, and O_2/He plasma oxidized GaN sample ($300^\circ C$, 0.3 Torr, 60 W and 30 min) was used as a reference sample for a thick pure GaO_x .

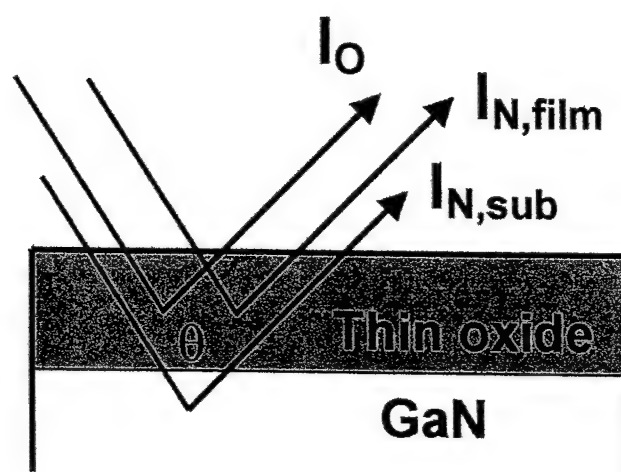


Figure 3 Schematic representation of thin RPAO oxide, or GaO_xN_y with non-negligible nitrogen content, on GaN substrate. When the nitrogen content in the oxide does not negligible, total intensity of N *KLL* (I_N) consists of i) intensity of N *KLL* from the substrate ($I_{N, \text{sub}}$) and ii) intensity of N *KLL* from oxide film ($I_{N, \text{film}}$).

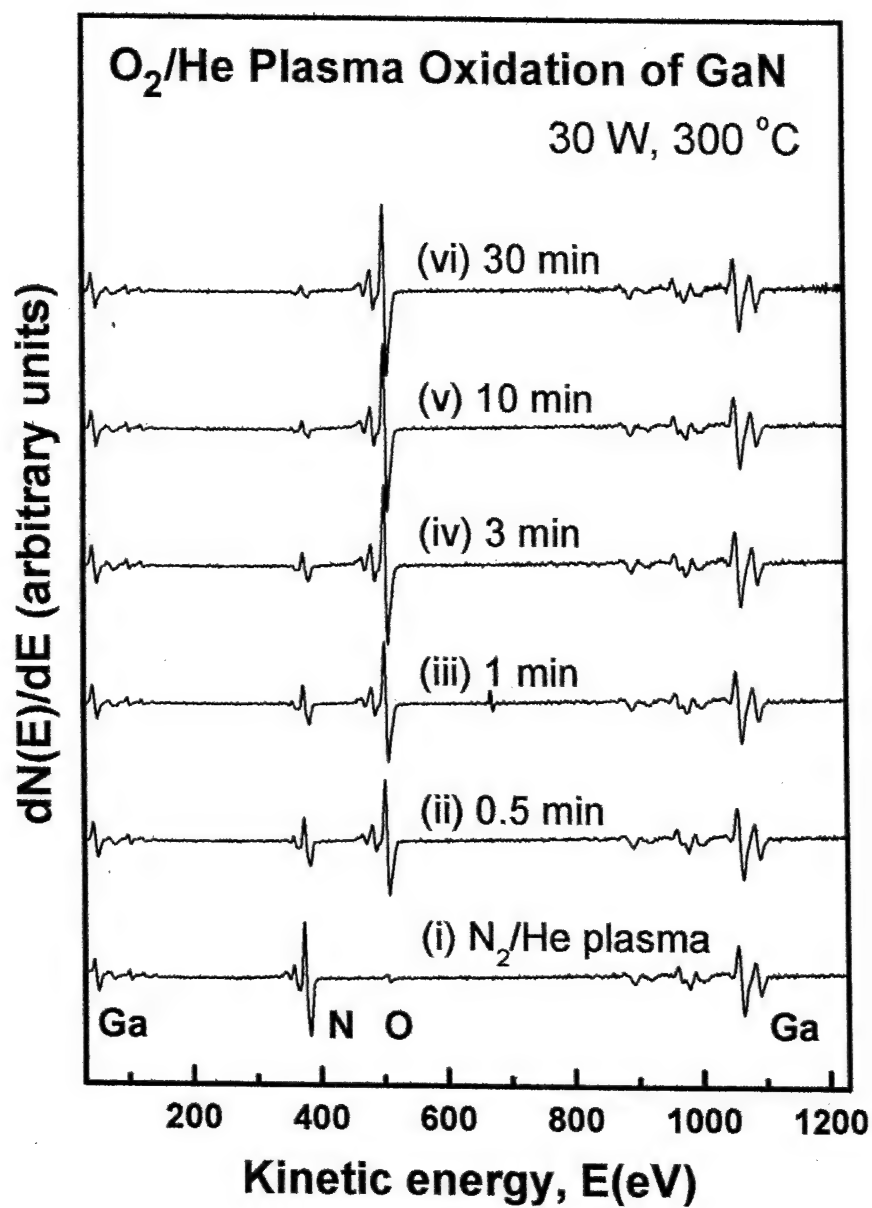


Figure 4 Time evolution of differential AES spectra from (i) N₂/He plasma cleaned GaN sample and (ii)-(vi) O₂/He plasma oxidation processing of GaN surface for 0.5 to 30 min.

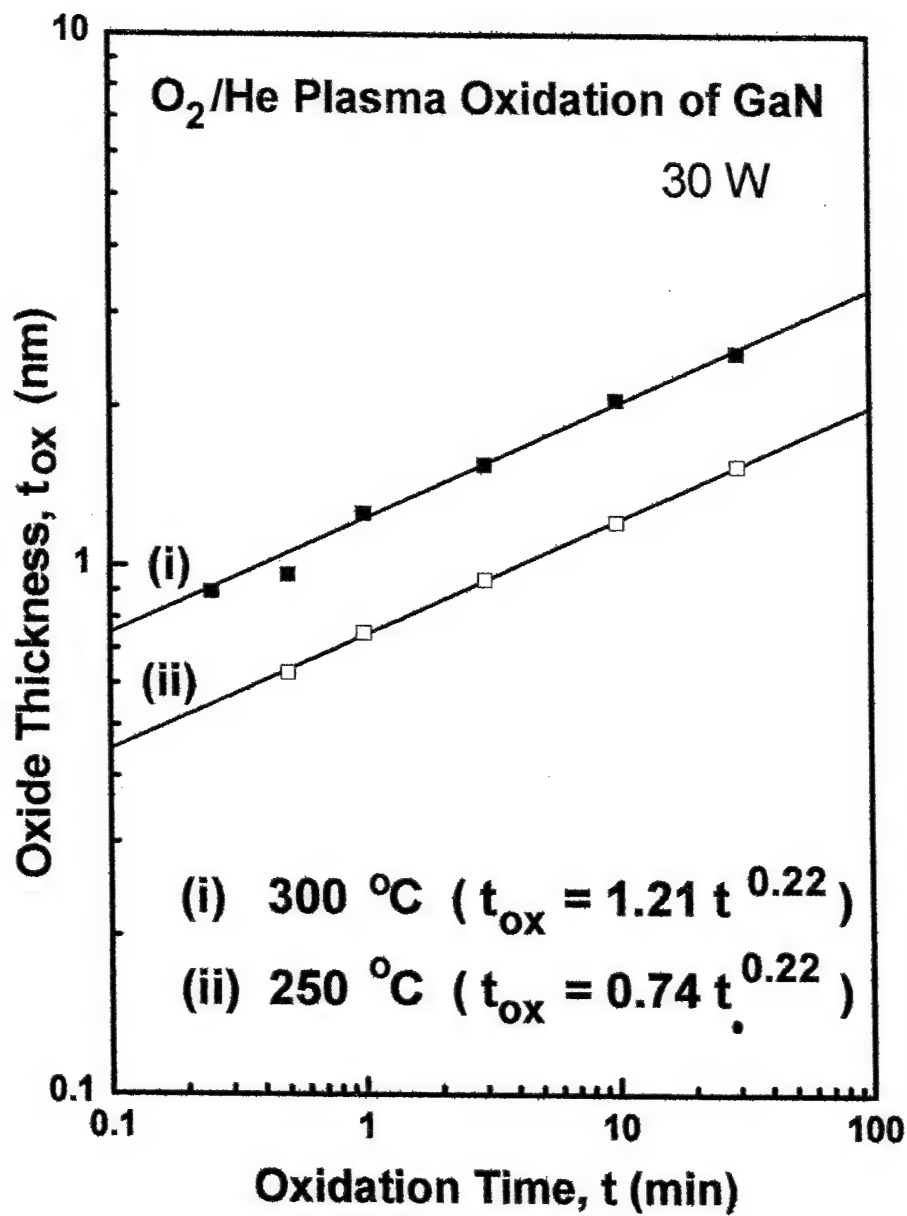


Figure 5 Log-log plots of the oxide thickness (t_{ox}) as a function of oxidation time (t) for the RPAO process using O₂ source gas at 250 and 300 °C, respectively. The straight lines connecting the data points represent a power-law dependence, i.e., $t_{ox} = \tau_o t^\beta$, where τ_o and β are fitting parameters. The oxide thickness is determined from Eq. (3) using I_O/I_N with an assumption of a homogeneous overlayer/substrate (GaO_x/GaN) system.

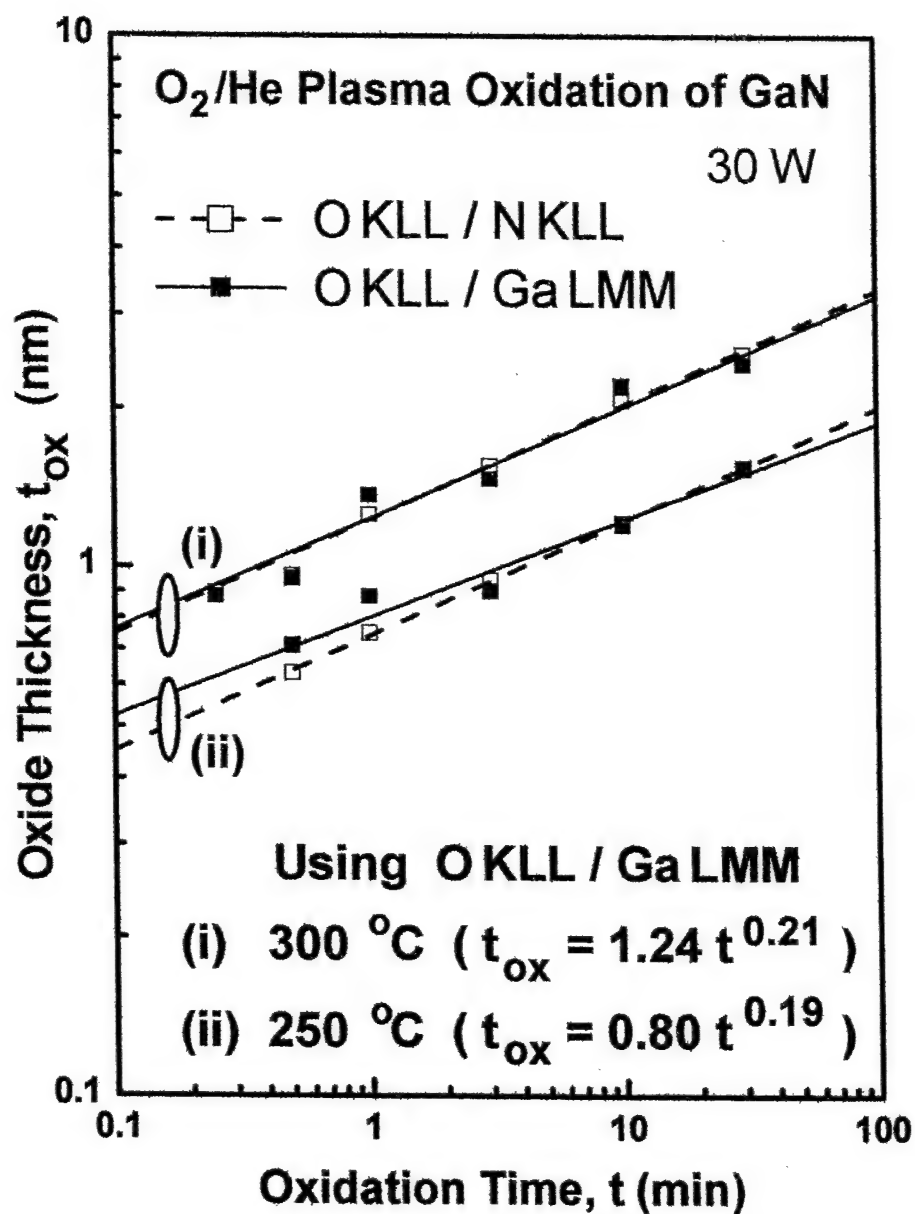


Figure 6 Log-log plots of the oxide thickness (t_{ox}), determined from Eq. (4) using I_O/I_{Ga} and taking λ_O as 1.14 nm, as a function of oxidation time (t) for the same RPAO process shown in Fig. 5. The oxide thickness and fitting data shown in Fig. 5 are also included as references.

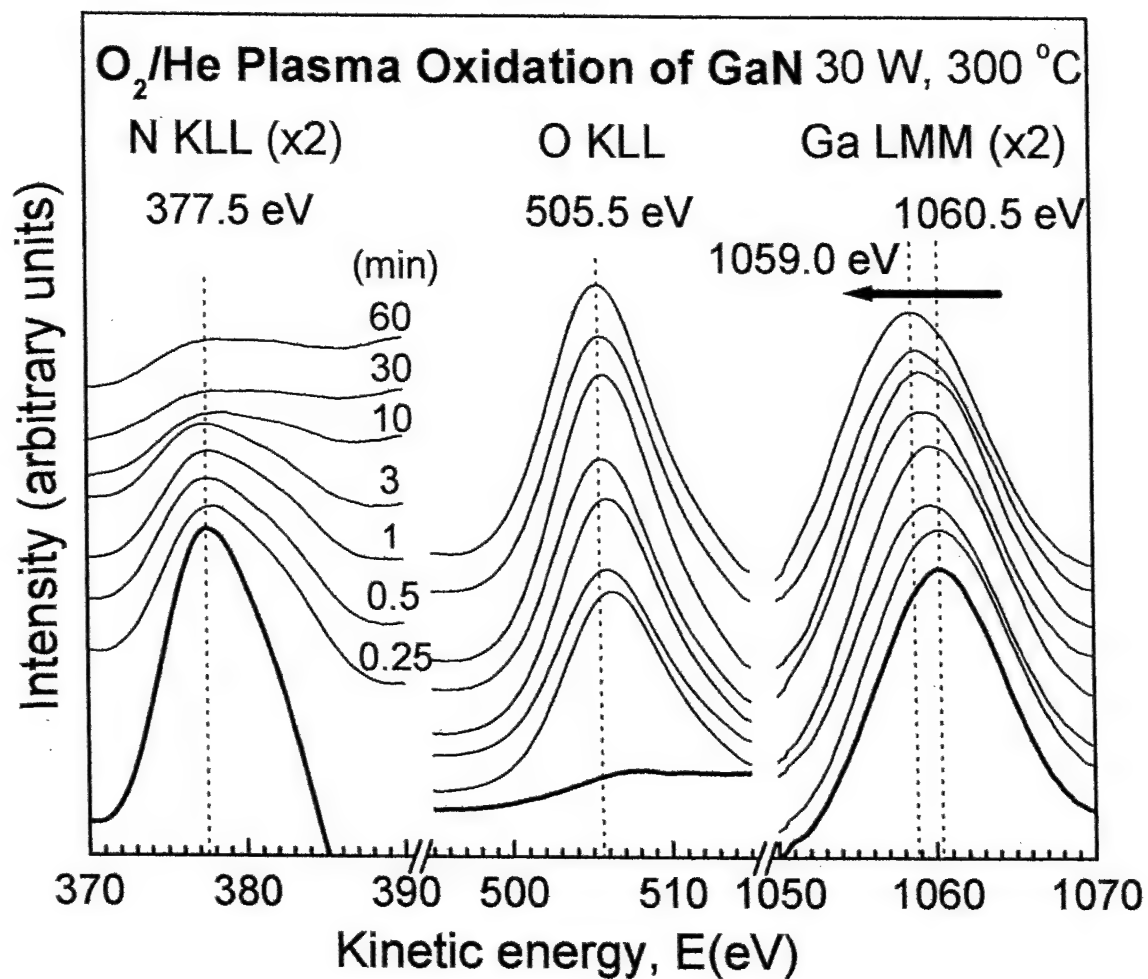


Figure 7 Time evolution of non-differential AES spectra from in-situ N₂/He plasma cleaned GaN sample and O₂/He plasma oxidation processing of GaN surface for 0.25 to 60 min.

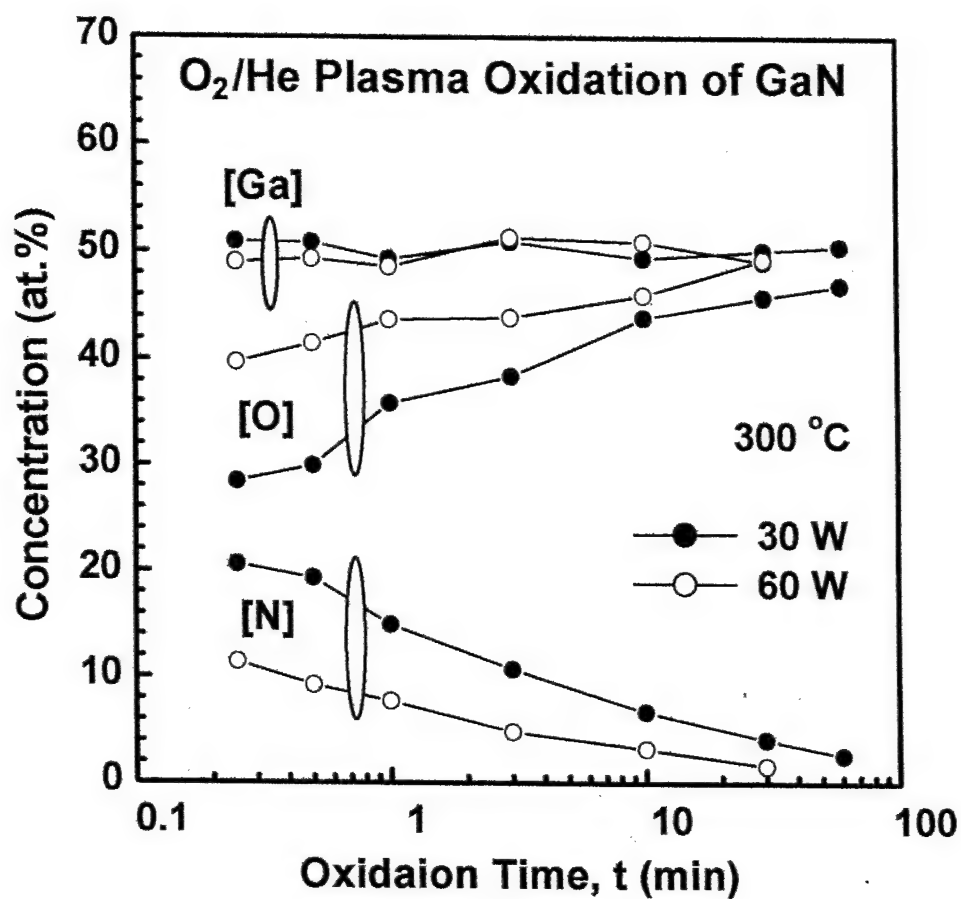


Figure 8 Relative change in composition of GaO_x as a function of nitridation time, where, $[\text{Ga}]$, $[\text{O}]$ and $[\text{N}]$ are Ga, O and N atomic fraction in the film (at. %).

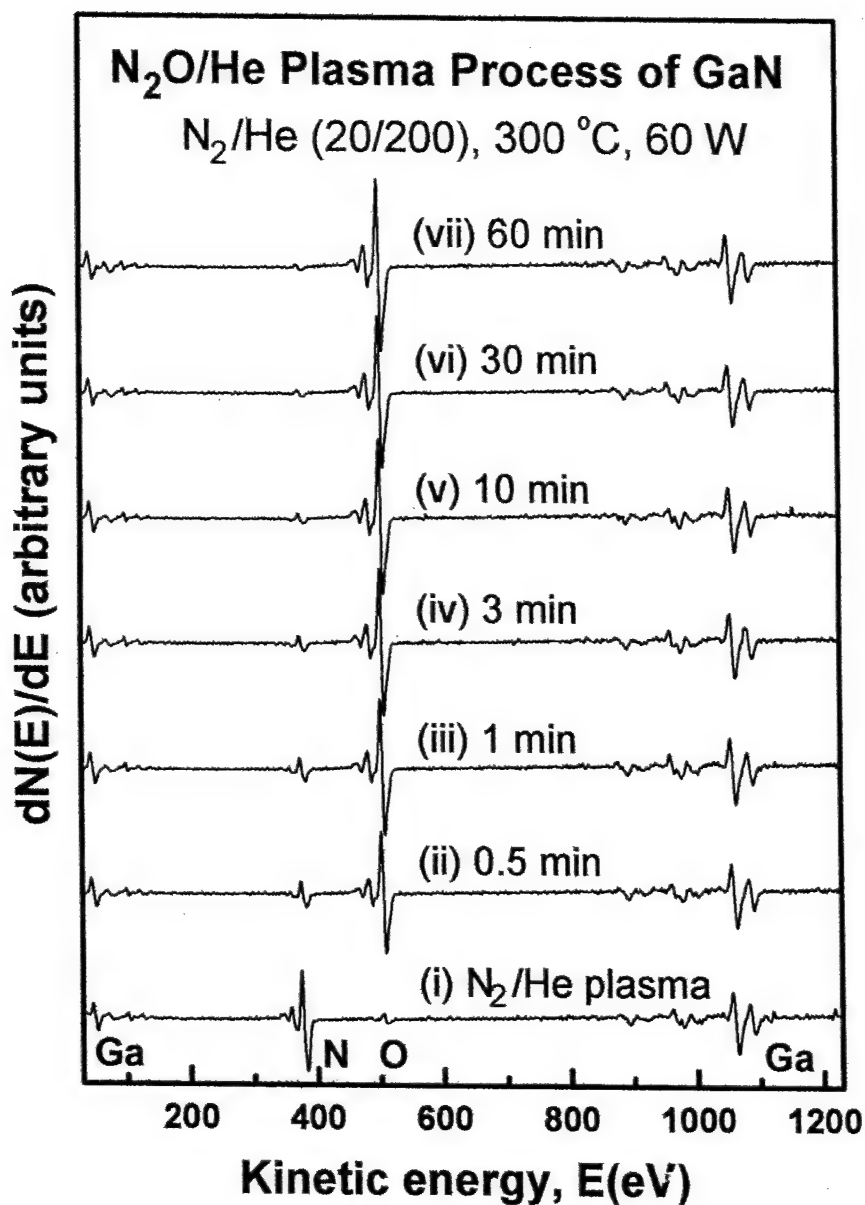


Figure 9 Time evolution of differential AES spectra from (i) N₂/He plasma cleaned GaN sample and (ii)-(vii) N₂O/He plasma oxidation processing of GaN surface for 0.5 to 60 min. The notation (20/200) in the figure refers to the flow rates of N₂O and He, respectively, in units of standard cubic centimeters per second (sccm).

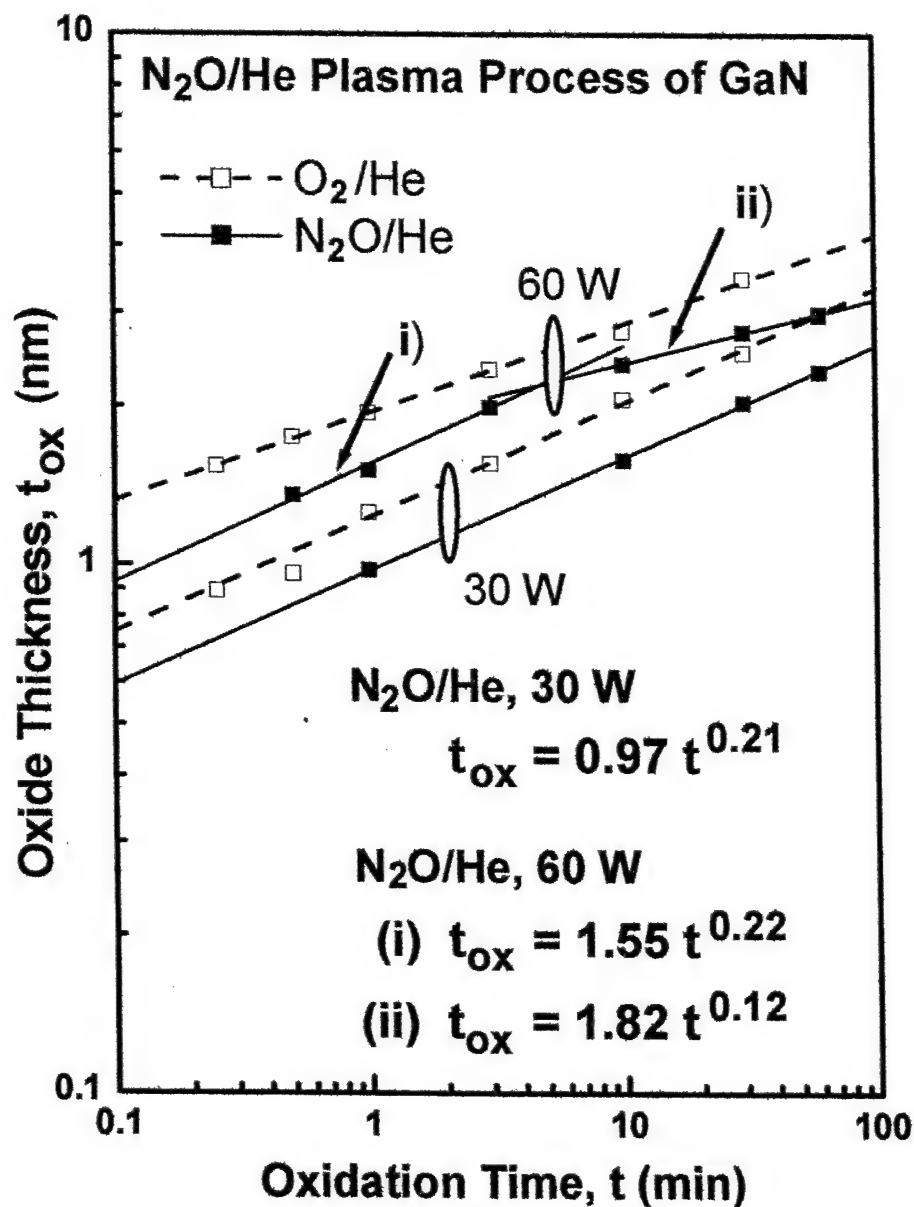


Figure 10 Log-log plots of the oxide thickness (t_{ox}) as a function of oxidation time (t) for the RPAO process using N₂O source gas at 300 °C with 30 and 60 W, respectively. The oxide thickness is determined from Eq. (3) using I_O/I_N . The oxide thickness and fitting data using O₂ source gas are also included as references.

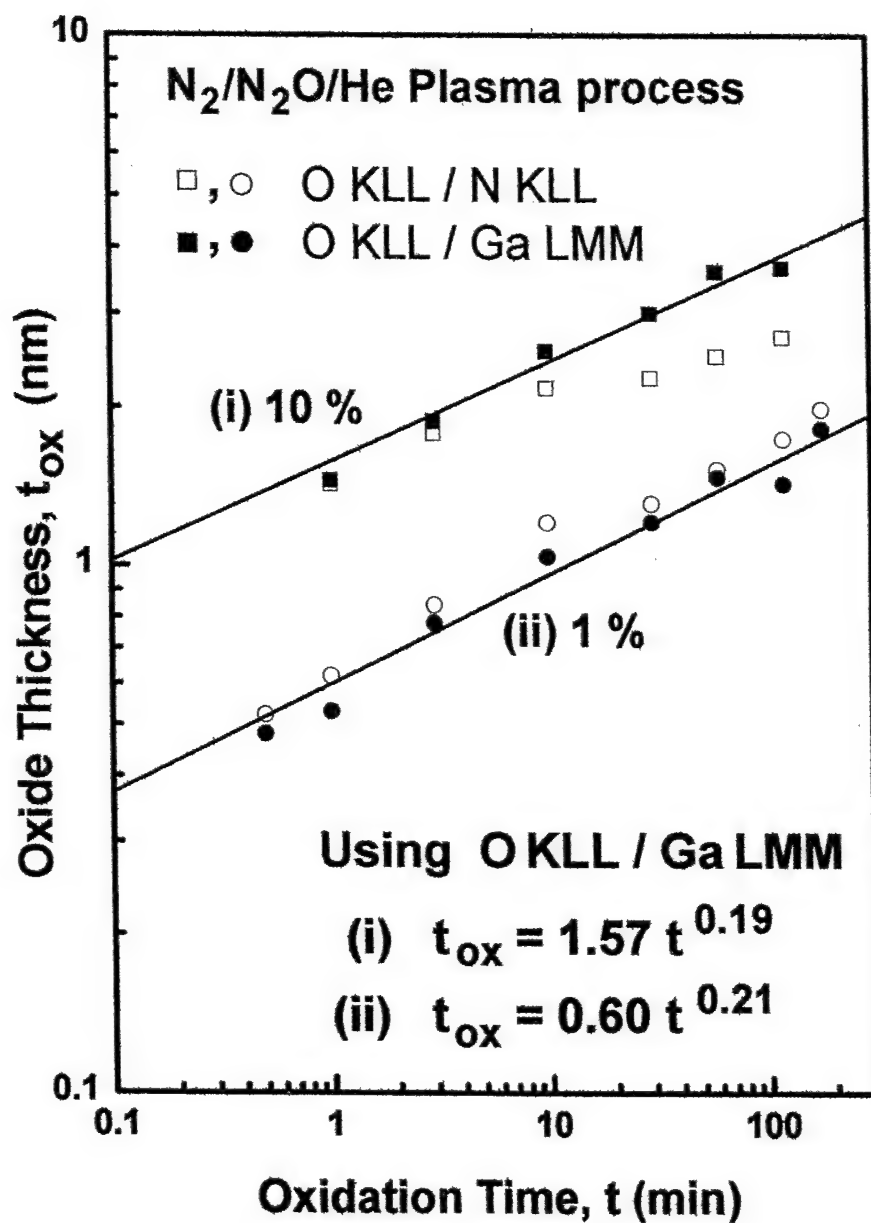


Figure 11 Log-log plots of the oxide thickness (t_{ox}), determined from Eq. (4) using I_o/I_{Ga} and taking λ_o as 1.14 nm as a function of oxidation time (t). The notation 10 % and 1 % in the figure refer to 10 % N₂O in N₂ and 1 % N₂O in N₂.

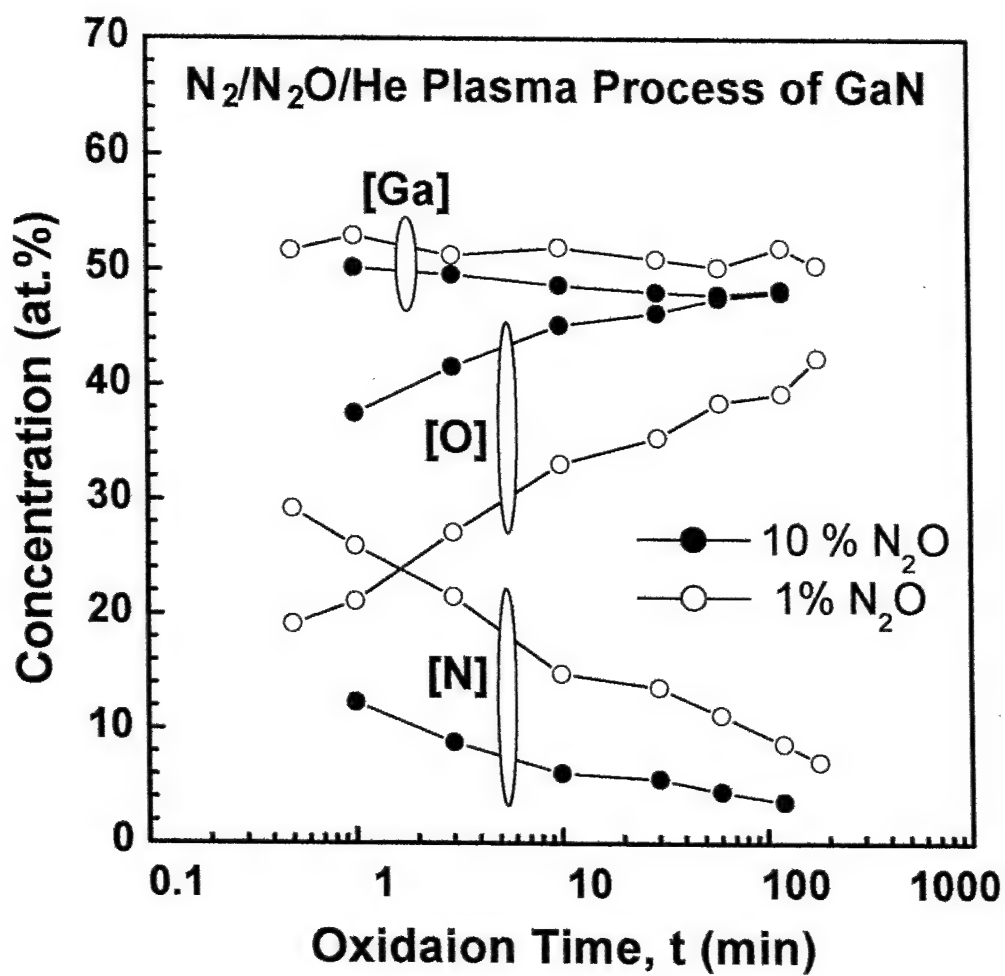


Figure 12 Relative change in composition of oxidized GaN sample as a function of oxidation time, where, [Ga], [O] and [N] are Ga, O and N atomic fraction in the film (at. %).

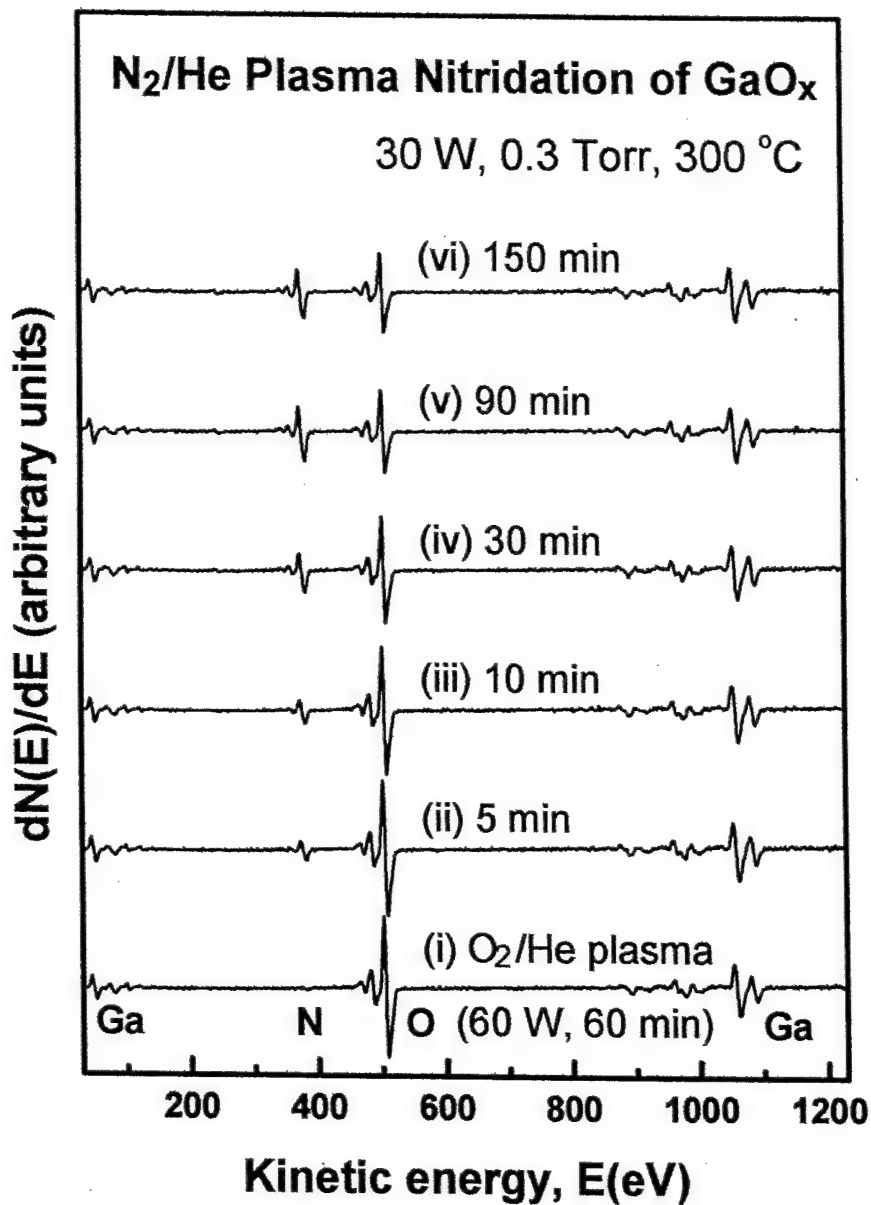


Figure 13 Time evolution of differential AES spectra from (i) O₂/He plasma oxidized GaN sample (GaO_x, ~3.5 nm) and (ii)-(vi) N₂/He plasma nitridation processing of GaO_x for 5 to 150 min.

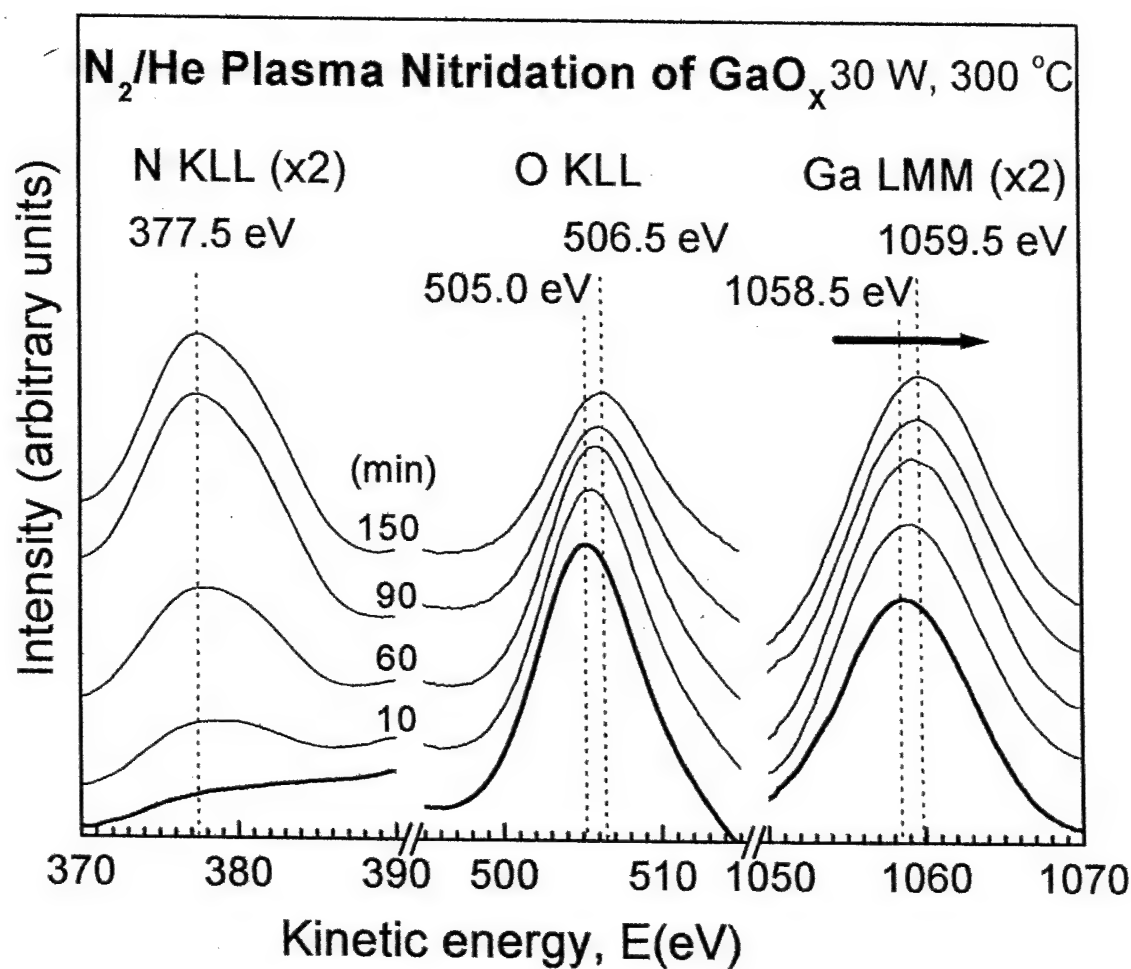


Figure 14 Time evolution of non-differential AES spectra from O_2/He plasma oxidized GaN sample (GaO_x , ~3.5 nm) and N_2/He plasma nitridation processing of GaO_x .

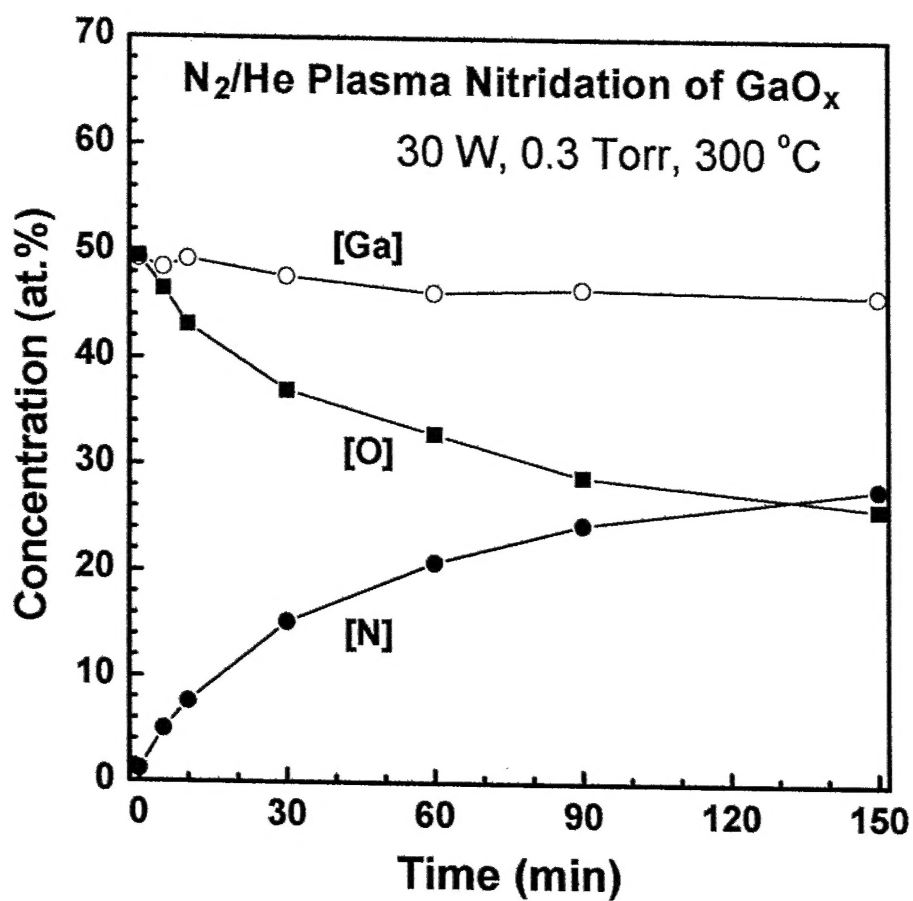


Figure 15 Relative change in composition of GaO_x as a function of nitridation time, where, [Ga], [O] and [N] are Ga, O and N atomic fraction in the film (at. %).

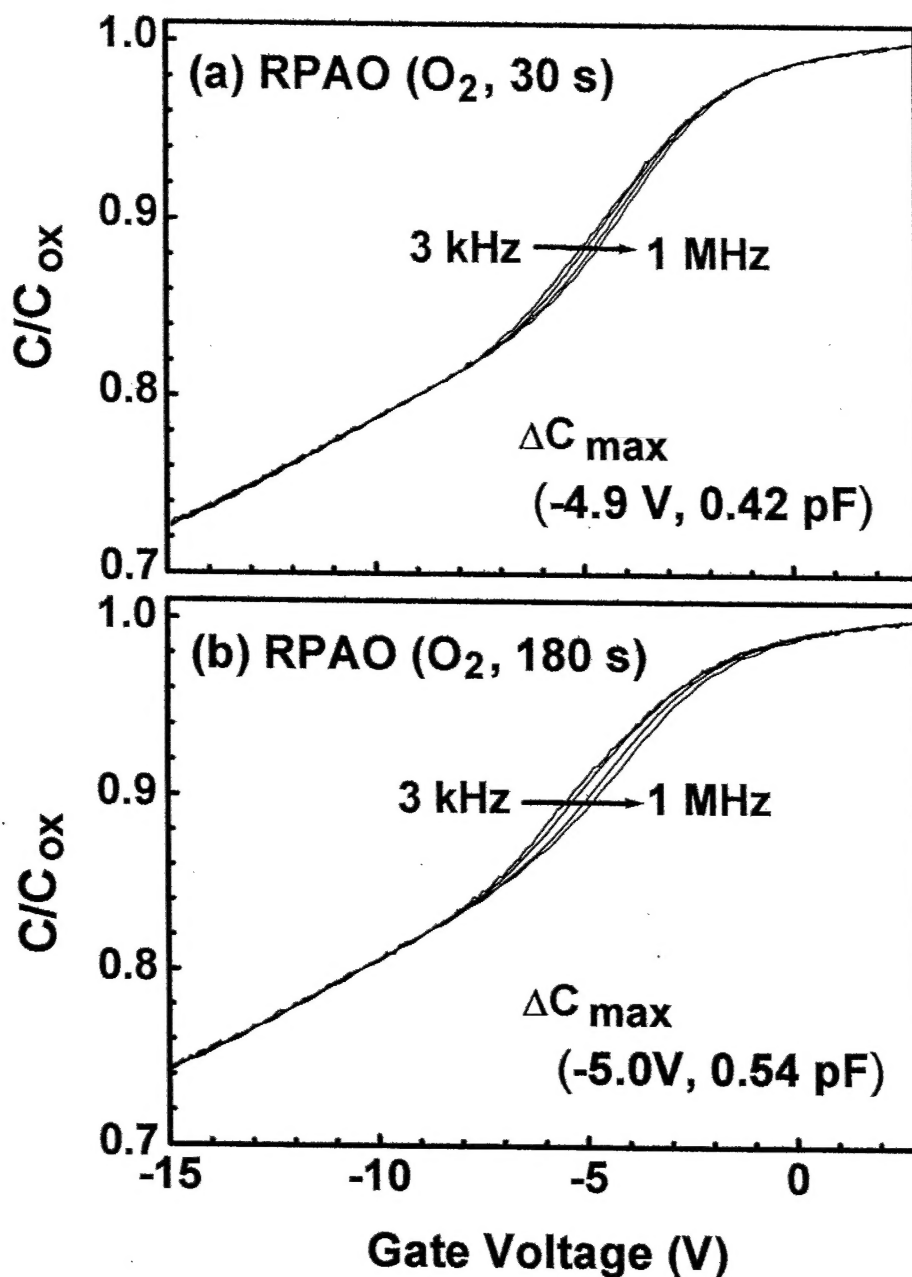


Figure 16 Frequency dependence (3 kHz, 10 kHz, 100 kHz, and 1 MHz) of the C - V characteristics of GaN MOS capacitors. The RPAO process using O_2 source gas was performed for (a) 30 s to obtain thin RPAO oxide of ~ 1.0 nm and (b) 180 s to obtain thin RPAO oxide of ~ 1.6 nm. The minimum D_{it} of each GaN MOS capacitor was determined at the gate voltage where measured C - V curves at 3 kHz and 1 MHz showed the maximum capacitance difference (ΔC_{\max}).

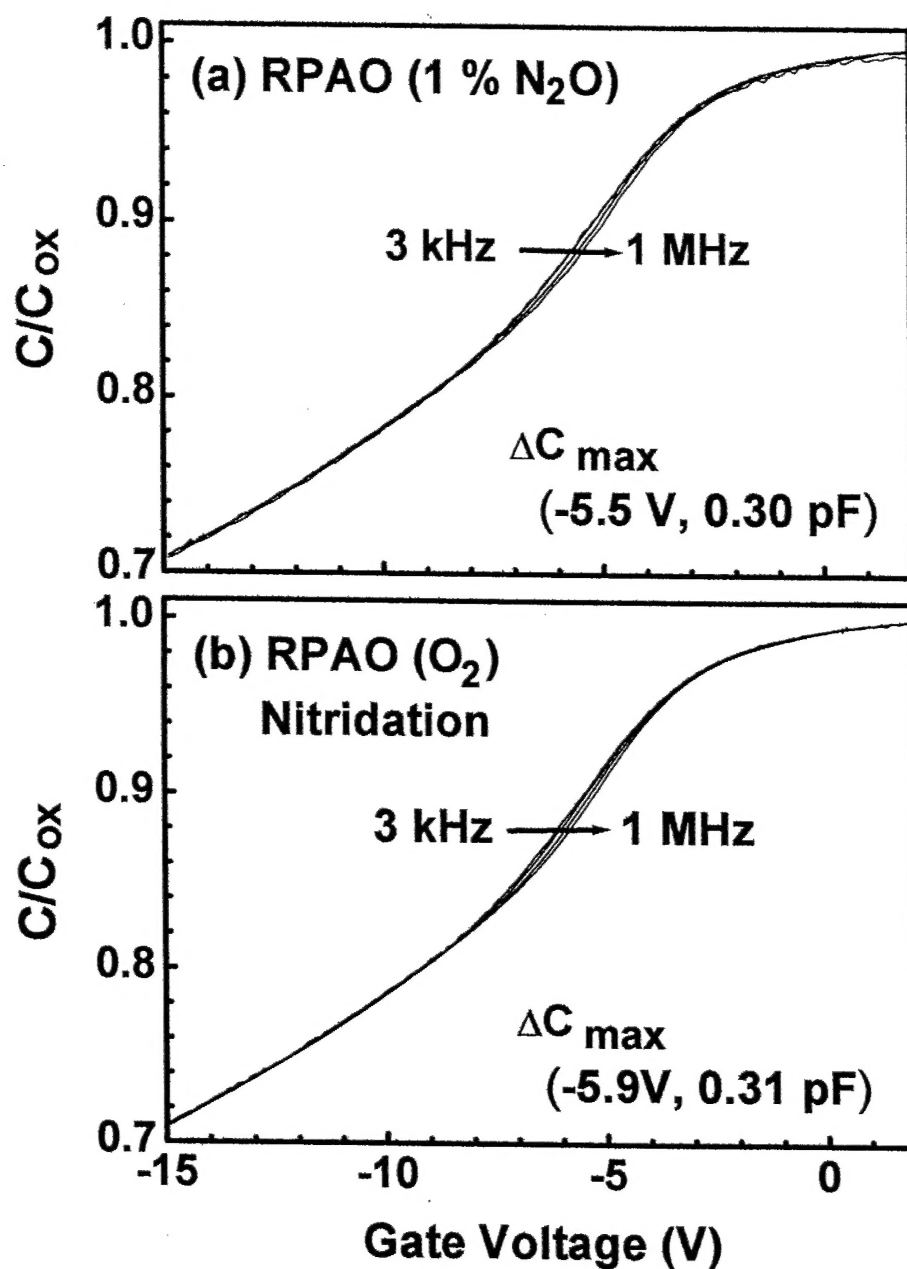


Figure 17 Frequency dependence (3 kHz, 10 kHz, 100 kHz, and 1 MHz) of the C - V characteristics of GaN MOS capacitors. (a) the RPAO process using 1% N_2O in N_2 source gas and (b) the RPAO process using O_2 source gas with followed nitridation using N_2/He plasma.

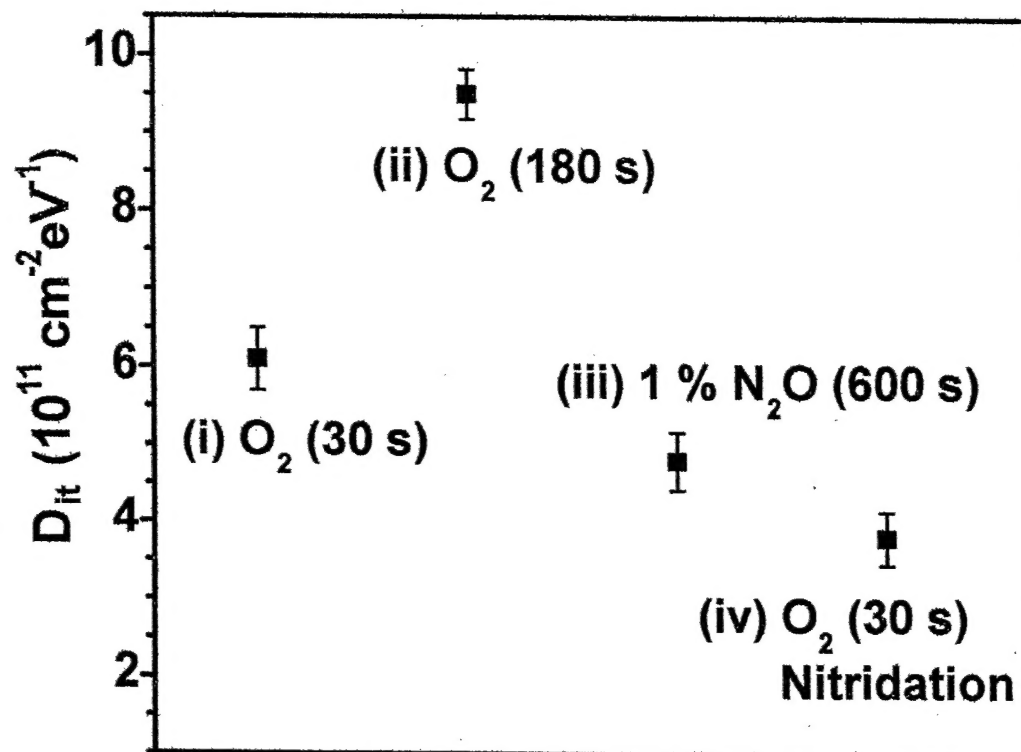


Figure 18 Minimum density of interface state (D_{it}) of GaN MOS capacitors with RPAO process using (i) O_2 source gas for 30 s, (ii) O_2 source gas for 180 s, (iii) 1% N_2O in N_2 source gas for 600 s and (iv) O_2 source gas for 30 s with followed nitridation using N_2/He plasma for 90 s.